DTRA Radiation Hardened Microelectronics Program: RH 90nm Technology Development Program

Presented at the Fault Tolerant Space-borne Computing Workshop

L.M Cohn/DTRA-RD

Lewis.Cohn@DTRA.MIL

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Agenda

- DTRA Radiation Hardened Microelectronics Program
- Boeing Radiation Hardening-by-Design (RHBD) 90nm Program
- Radiation Hardening by Process (RHBP) Programs
  - BAE Systems 90nm RHBP Program
  - Honeywell 90nm RHBP Program
- RH Enabling Technology Development Projects
- Summary

RHM Program Technology Development Program Hierarchy

Pyramid level	Technologies
RH P&Q Program (AF SMC Funded)	RH 16Mbit SRAM RH SERDES RH 150nmLibrary RH FPGA
RH Development & Demonstration Task	**RHBD 90nm Demonstration** RHBD UDSM Demonstration RH A/M-S Technology Demonstration RH non-volatile FPGA Demonstration
RH Enabling Technology Development Task	**RH 90nm Process Development** RH EDA & TCAD RH Modeling & Simulation SEE Mitigation RHA
Commercial Microelectronics Technology	Baseline Technologies

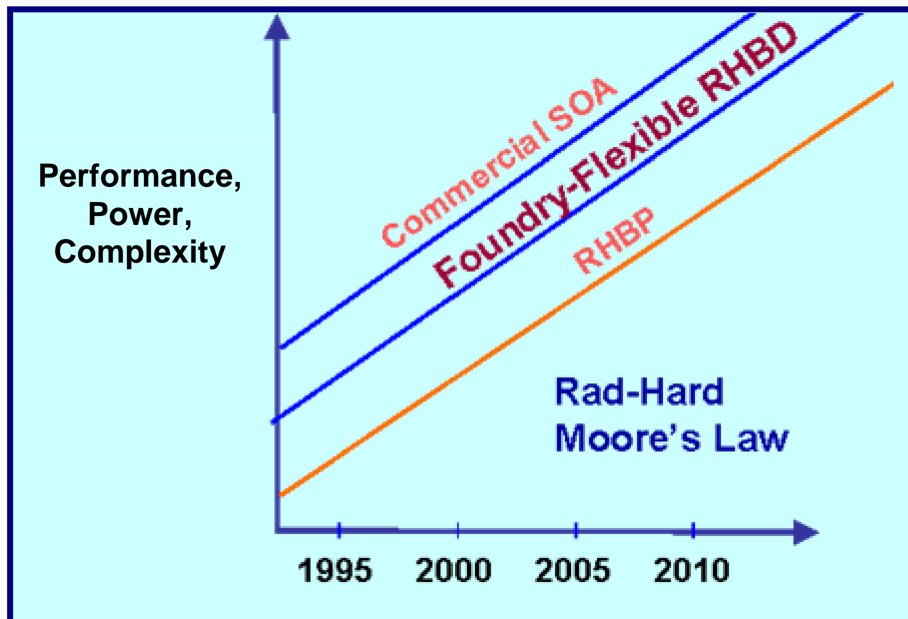
DTRA/DARPA Boeing RHBD 90nm Program

RHBD 90nm Technology Development & Demonstration Program

- Program Objectives
- Program Description
- Scope of Work
- Program Organization
- Major Accomplishments
- Technology Transfer Activities
- Summary

RHBD Program Objectives

- Develop and demonstrate a 90nm RHBD technology approach to provide strategic rad hard performance with a < one generation SWaP penalty
  - High performance, low power
  - Leverage supported IP & tools
  - Foundry Flexible - Assured sources



Hardness Targets	
Total Ionizing Dose	> 2 Mrad(Si)
Single Event Upset	< 1E-10 errors/bit-day (Adams), LET_{Th} > 20
Single Event Latchup	LET_{TH} > 120 Mev-cm^2/mg
Dose-Rate Upset	>1E10 rad(SiO_2)/sec

Acceptable RHBD Penalties	
Area	≤ 2X
Speed	≤ 1.5X
Power	≤ 1.5X

RHBD Phase 2 Program Goals & Requirements

Radiation Requirements

Parameter	Goal	Requirement
Total Ionizing Dose (Mrad(Si))(4)	> 2	> 1
Single-Event-Upset (errors/bit-day)(1)	< 1E-10 LET > 20	< 1E-10 LET > 15
Single-Event-Latchup (LET in Mev-cm^2/mg)(2)	> 120	> 100
Neutron Irradiation (Mev eq. n/cm^2)	> 1E13	>1E12
Dose-Rate Upset (rad(SiO$_2$)/sec)(3)	> 1E10	> 1E 9
Dose-Rate Survivability (rad(SiO$_2$)/sec)(3)	1E12	1E 12

Generic Trades

- Component-Level
- Chip-Level

Categories	Area	Power	Speed
Logic	~1X	~1X	~1X
Flip-Flops	<2X	<2X	~1X
SRAM	<4X	<2X	~1X
Mixed-Signal	~1X	~1X	~1X

Actual area trades based on RHBD Phase 2

Memory + Logic = 2X

*One Generation Chip-Level RHBD Area Penalty = (2X)(0.5) + (3X)(0.2) + (1.2X)(0.3) = 2X

(Memory) (Flip-Flops) (Gates)

RHBD Program Overview

2004	2005	2006	2007	2008	2009

Proved Efficacy
SRAM Penalty >1 Gen.

Transition to 90nm
SRAM Penalty <1 Gen.

Confirm Efficacy for 90nm Circuits

Demonstrate RHBD on Complex and Large Circuits

Phase 1 | **Phase 1.5** | Phase 2

130nm Test Chips

- RHBD Techniques
- Digital cells
- SRAM
- Discrete transistors

90nm Quick Chip

- RHBD Techniques
- Discrete Transistors

90nm (9LP) Test Chip

90nm (9SF) Test Chip

- Multiple RHBD Techniques
- SRAM
- Digital
- Analog
- IP

90nm Initial RHBD Test Circuits & Library

- Complex RHBD Test Circuits
- Pre-Phase 2 Library

Complete Rad Hard 90nm Library & Design and Fab Demonstration Chip

DARPA Funded

DARPA/DTRA Funded Under MOU

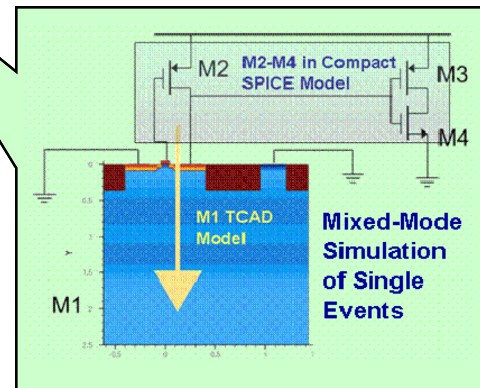
Scope of Work

- RHBD Design Techniques Characterization
- 90nm Libraries & IP Development and Optimization
- SEE Analysis methods & tools
- TCVs, CTVs
- PDVs – Demonstrations fabricated and Characterized
- TRL “TBD” Design Capability
- 65nm and 45nm preliminary investigations

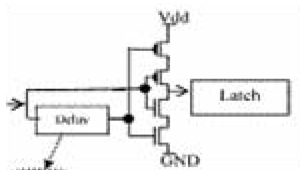
RHBD Approach

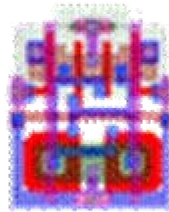
- Non Invasive RHBD Techniques
- Mixed Signal CMOS
- Foundry-Flexible Library & IP
- Mixed Physical/Electrical Analysis
- Characterization Circuits
- Commercial IP Hardening
- RHBD SOC Design Flow
- SOC Pathfinders/Demonstrations

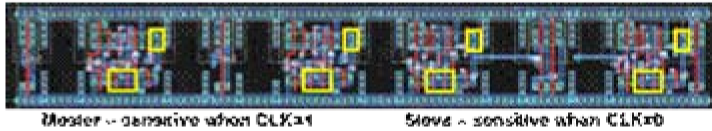
- **Process Option Selections**
- **Design Rule Waivers**
- **Device Layout & Placement**
- **Circuit Topology**
- **Architecture**



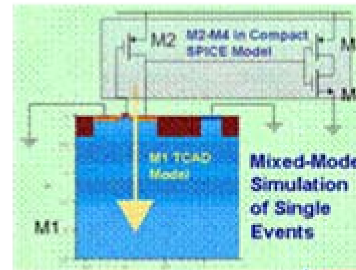
RHBD Program Tasks

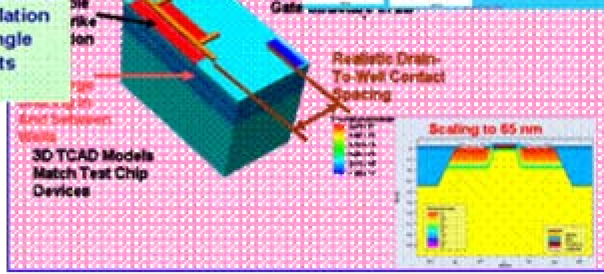


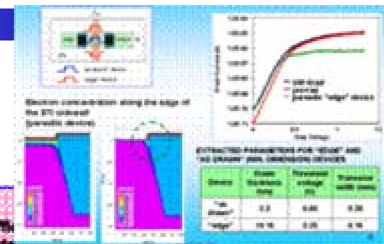




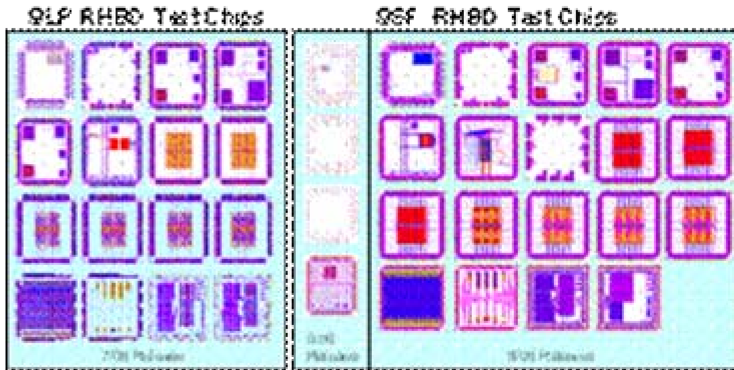
Mitigation Techniques



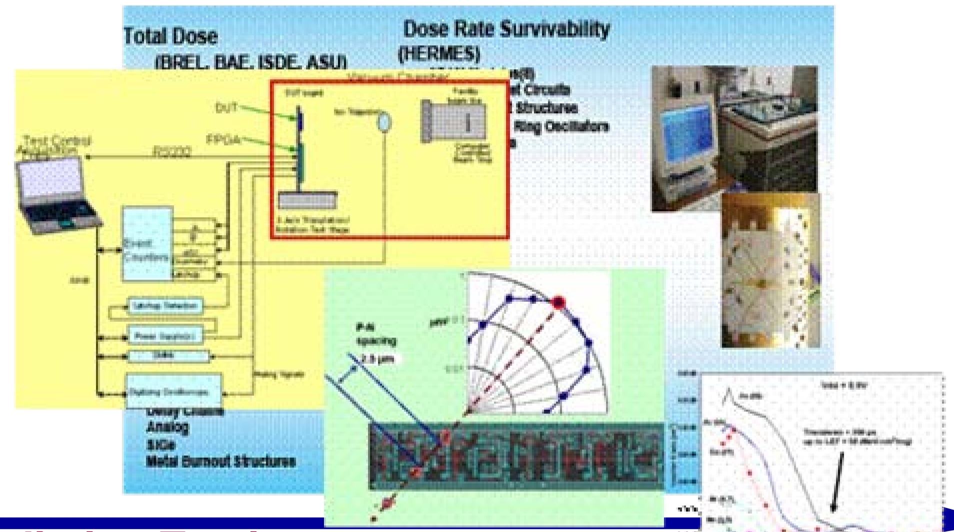




Analysis Methods



Test Chips



Radiation Testing

RHBD Program Tasks

Development Step	Data included
Synthesis	• **Liberty Format Files (.lib)** • **Synopsys Data Base Files (.db)**
Simulation	• **Verilog simulation models** • **VHDL VITAL simulation models** • **Cadence schematics**
Placement & Routing	• **Cell physical geometry** • **Cell frame views** • **Cell timing views** • **Cell power views** • **Technology file**
Verification	• **Cell SPICE netlist** • **Verification decks version**
Support data	• **Cell datasheets** • **Models & Design rules version**

ASIC Design Tools

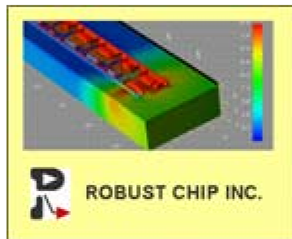
RHBD Libraries & IP

Chip-Level SEE Analysis

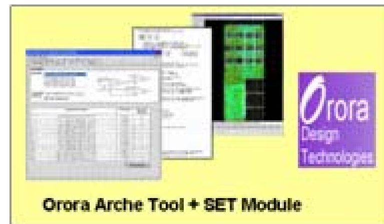
Demonstration RH SOC's

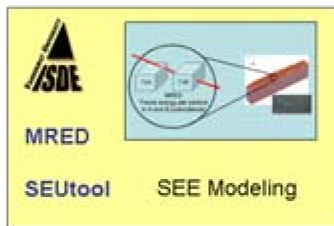
RHBD Program Tasks

Analysis, Models & Tools

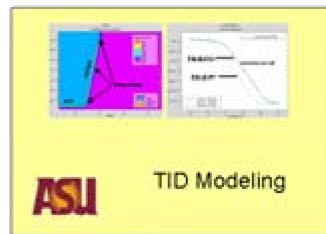


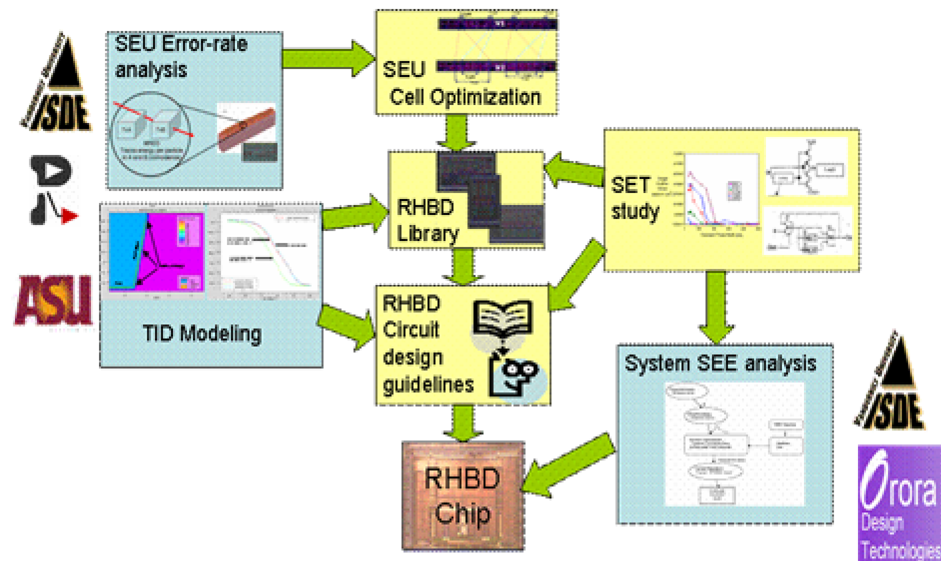
Fast Design-Time analysis tools





In-depth analysis of advanced technology





Major Accomplishments

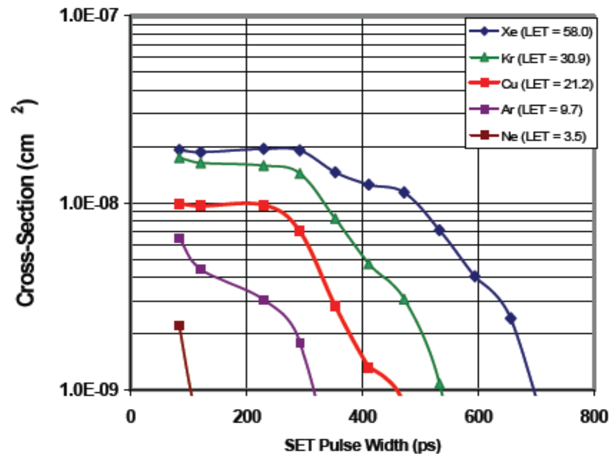
- Technology Characterization
  - V3 DICE SEU Characterization completed
  - Robust Chip Mixed-mode TCAD grazing angle study
  - ISDE
    - DICE SEU rate in space calculation
    - SET analysis tool
  - Taped out
    - V4 DICE
    - SET Generation & mitigation test chip
  - Designed SET pulse broadening test chip
  - Proton testing at IU & LBL (SRAM, PLL)
    - MRDC SRAM passed
    - PLL does not upset
    - More tests planned (energies, angles)

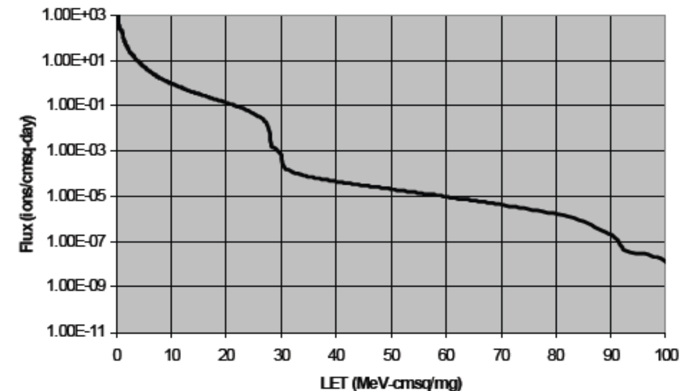
Major Accomplishments

- Design Enablement
  - Clock Generation PLL test & evaluation complete (electrical, TID, Dose Rate, SEL, SEU) – all requirements except SEU met
  - Taped out
    - PDV1 SRAM at-speed SEU test chip
    - SERDES critical sub-circuit blocks
    - LVDS Transmit & Receive
    - V2 I/O Library (meets JEDEC specs, suports C4, improved drive, ESD)
    - SSTL Test-chip
    - Programmable PLL
  - Completed
    - DDR2 controller (synthesized block)
    - SERDES Receiver
    - SERDES Test Methodology
- Demonstrations
  - PDV2
    - Selection completed
  - PDV1
    - CDR 3/28 for 4/7 tape-out - Completed

SET Test Results

- We have successfully designed, fabricated, tested and characterized SET pulse widths for common combinational logic elements
  - The largest transients observed with Xenon (LET 58) were < 800ps at 0.9Vdd
- SET Rate is strongly dependent on transient pulse width
  - Pulse width increases with increasing LET
  - Space environment heavy ion flux falls off exponentially with increasing LET





- SET mitigation based on temporal redundancy requires that the delay be longer than the transient that the circuit is required to reject.
- We must sufficiently limit SETs to meet requirements, not eliminate them!

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SET & TID Test Results

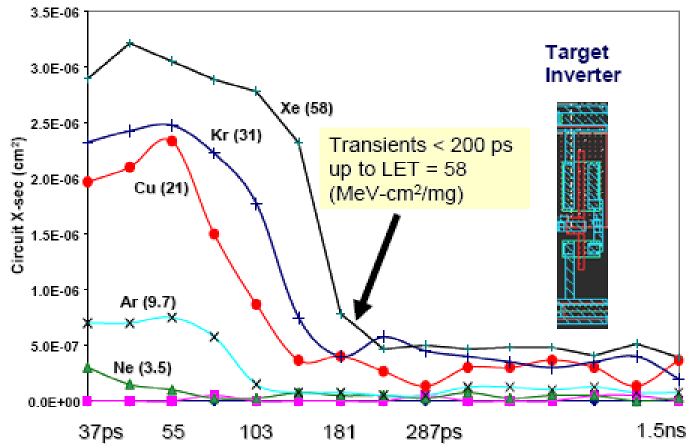


Figure 7. Typical Single event transient pulse widths

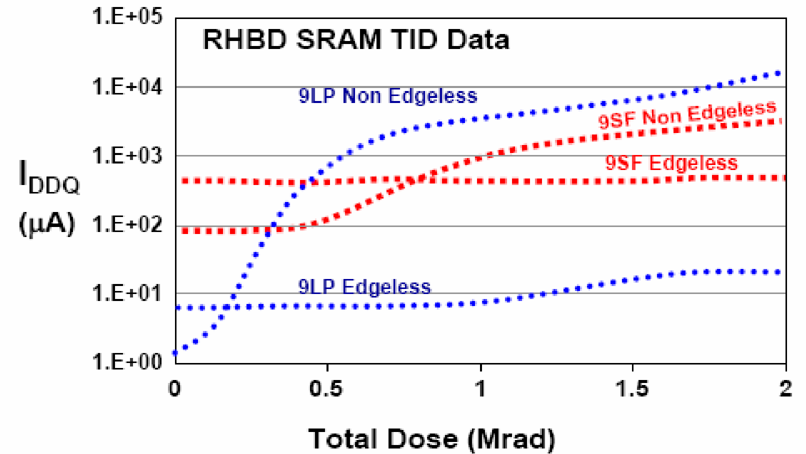


Figure 2. SRAM TID Leakage Current Results

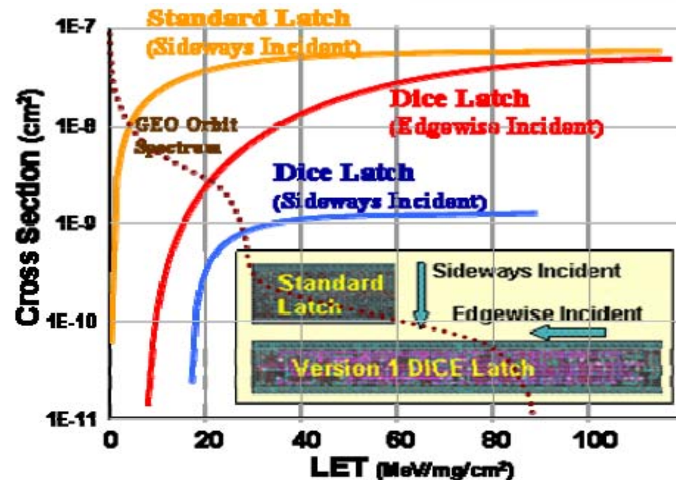
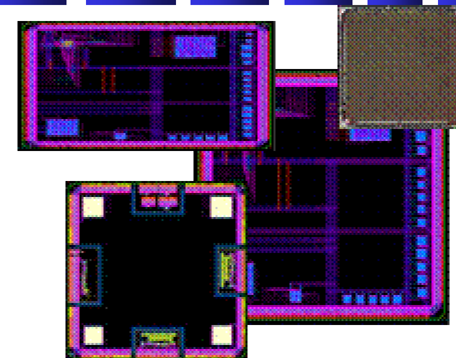


Figure 4. Latch SEU Cross-Sections (60^0 Incident Beam)

Standard Cell Libraries

- 1014 Cells - equivalent to commercial library with parameterized options for speed, power, radiation hardness.
  - Status V1 Library Status
    - Electrical, Functional, Radiation characterization complete
    - EDA views, models validated
    - Used in multiple circuit designs
    - SET generation and sensitivity characterization in work
  - DICE Status
    - V2 – Passed Go-NoGos, mitigated angular effects
    - V3 - Jan ‘08 Test – Used on OPERA/PDV1
    - V4 – May ‘08 Test



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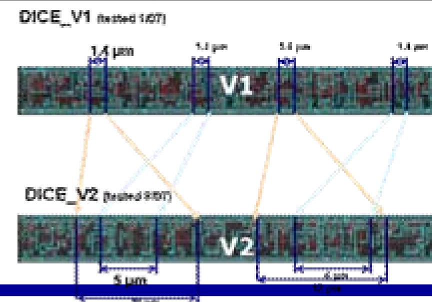
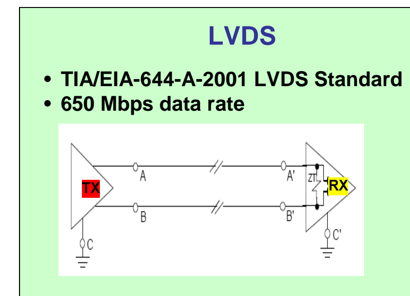


Input/Output (I/O) Macro-cell Library

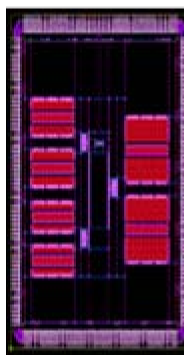
- Robust General Purpose I/O Library
  - Wire-bond and area array/flip-chip
  - Status
    - V1 tested and successfully used in multiple test chips
    - V2 Test Chip released to TAPO 1/28
- LVDS I/O
  - High-speed (500 MHz) and low jitter I/O
  - Status:
    - Transmitter test chip released 10/22/07 parts 3/26/08
    - Receiver test chip released 1/28/08
    - Integrated test chip release 4/7/08

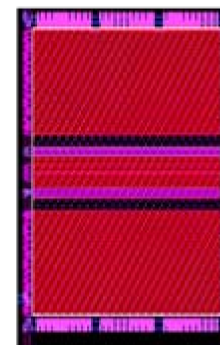
- Input
- 3-state Output (9mA, 18mA)
- Output (9mA, 18mA)
- Bidirectional (9mA, 18mA)
- I/O Power/Ground
- Core Power/Ground
- Bare Wire (No ESD)
- Analog (ESD only)
- Corner



1Mrad Static Random Access Memory (SRAM)

- **Status:**
  - **At speed SRAM test chip released 7/2/07**
    - **in electrical test**
  - **OPERA SRAM test chip released 1/28/08**
    - **OPERA will use three SRAM configurations:**
      - **1K x 72**
      - **256 x 72**
      - **64 x 72**





Phase Locked Loop (PLL) Macro-cell Library

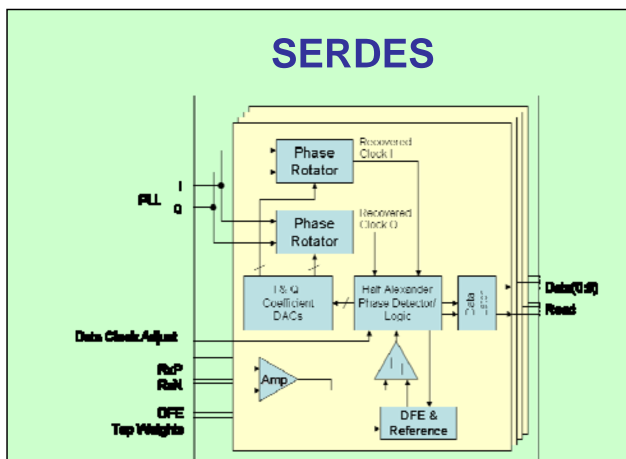
- Configurable, clock-generation PLL
  - Electrical test complete - met all requirements
  - Conducting SEE test now
- DDR2 Interface PLL
  - Tapeout 10/22/07
- SERDES IF PLL
  - Tapeout 4/7/08

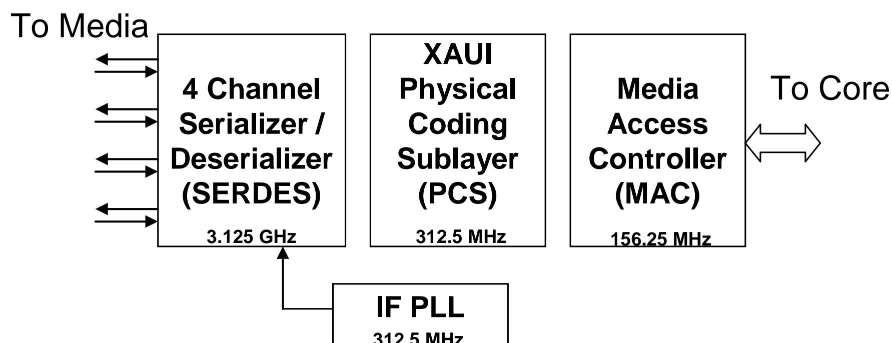
PLL

Integrated Analog-Charge Pump PLL Architecture

SERIALIZER/DESERIALIZER (SERDES) High Speed Data Transfer Macro-cell Library

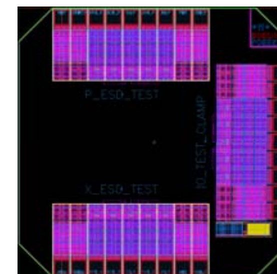
- 10Gbps Ethernet (using XAUI)
  - SERDES plus synthesizable components
- Status
  - Critical SERDES subcircuits on 1/28/08 tapeout
    - Transmitter driver
    - Receiver amplifier
    - Phase rotator
  - High-speed test methodology established

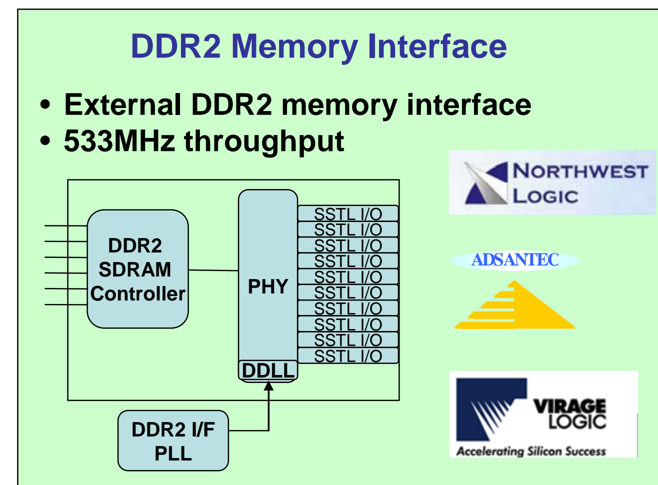




Dual Data Rate (DDR2) Interface Macro-cell

- High-bandwidth interface to external storage
  - Series Stub Terminated Logic (SSTL) I/O pad - hard macro
  - Physical Layer (PHY) – hard macro
  - Controller - synthesizable
  - PLL (hard macro)
- Status
  - SSTL I/O Design tapeout 1/28/08
  - PHY development contract – 2/14/08
  - PHY test chip tapeout April, 2008



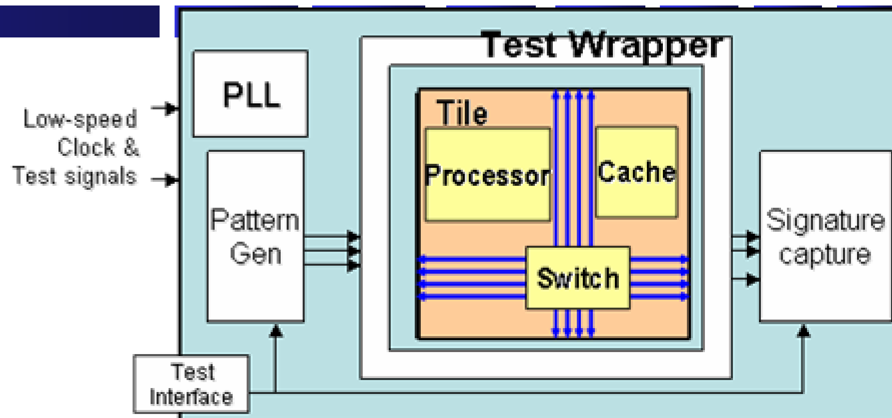


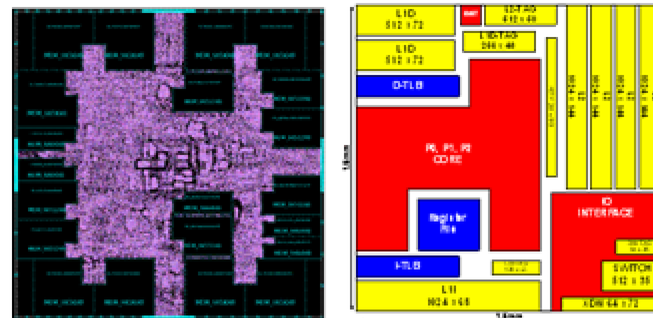
SDRAM interface circuit

PDV1 – OPERA

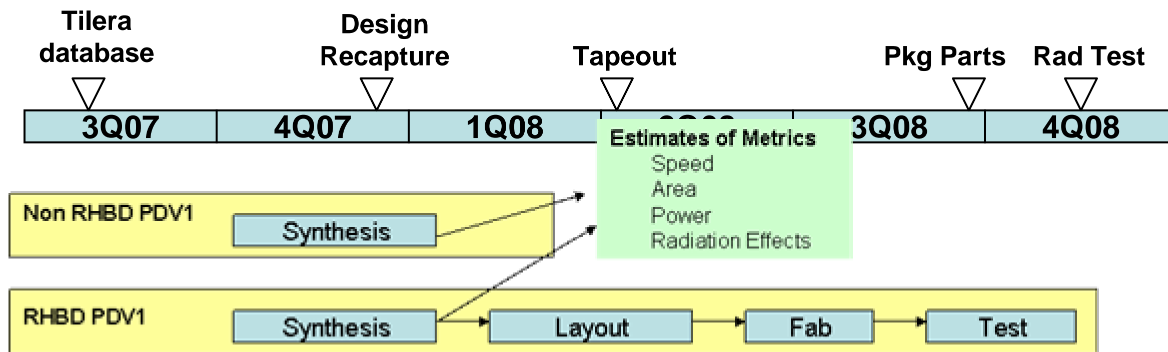
(Single Tile from Multi-Core 70GOP Processor)

- MAESTRO Tile (minus FPU)
- On track for TAPO 4/7/08 tapeout
- Meet all requirements except for the 480MHz
  - Methods identified to improve speed for PDV2/MAESTRO



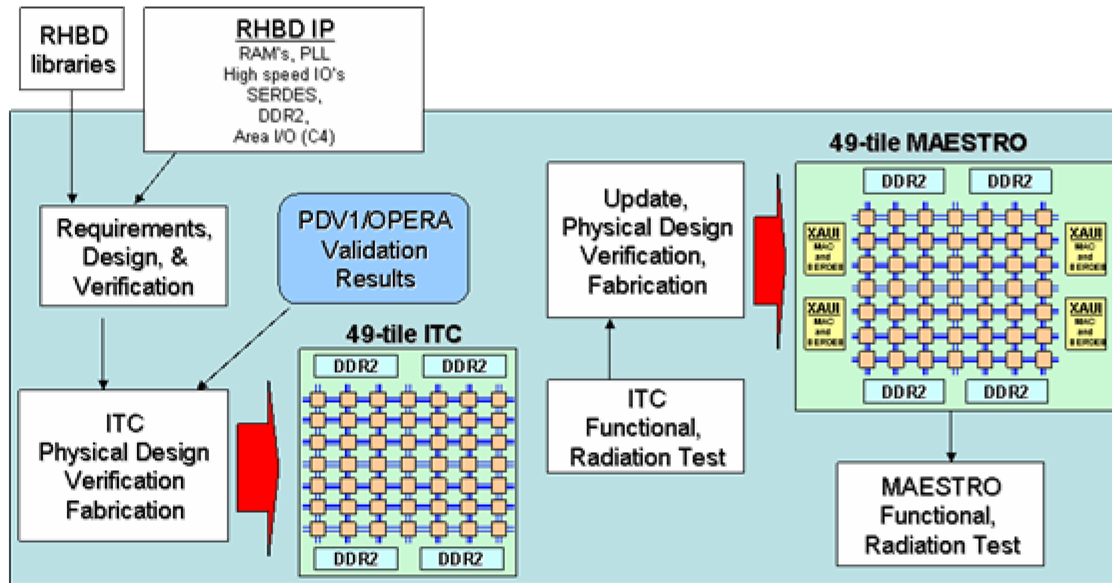


Category	Value
Radiation	1Mrad (see rad reqs chart)
	SEE at-speed memory BIST
	SEE at-speed Scan
	SEE at-speed Functional
Power	270mW
Speed	480MHz
Area	5 X 5 mm
Temperature	-40 to 125C
Voltage	1.0 V ± 5%
IO Speed	< 100MHz
I/O Count	< 500



MAESTRO

- Separate Program – First Application
- 70 GOP/GFLOP Multi-Core Processor with Data Communication Mesh



Requirements	
Number of Tiles	49
Clock F (MHz)	480
Cache Size	4 Kbytes
Die Size	22X22 mm
TID	500 krad
SEU[1]	2.4E-11 E/bit-day
SEL	No Latchup LET < 100
SET	>97% eliminated
Power	28W
Op temp	-40C t0 125C
GOPS	71

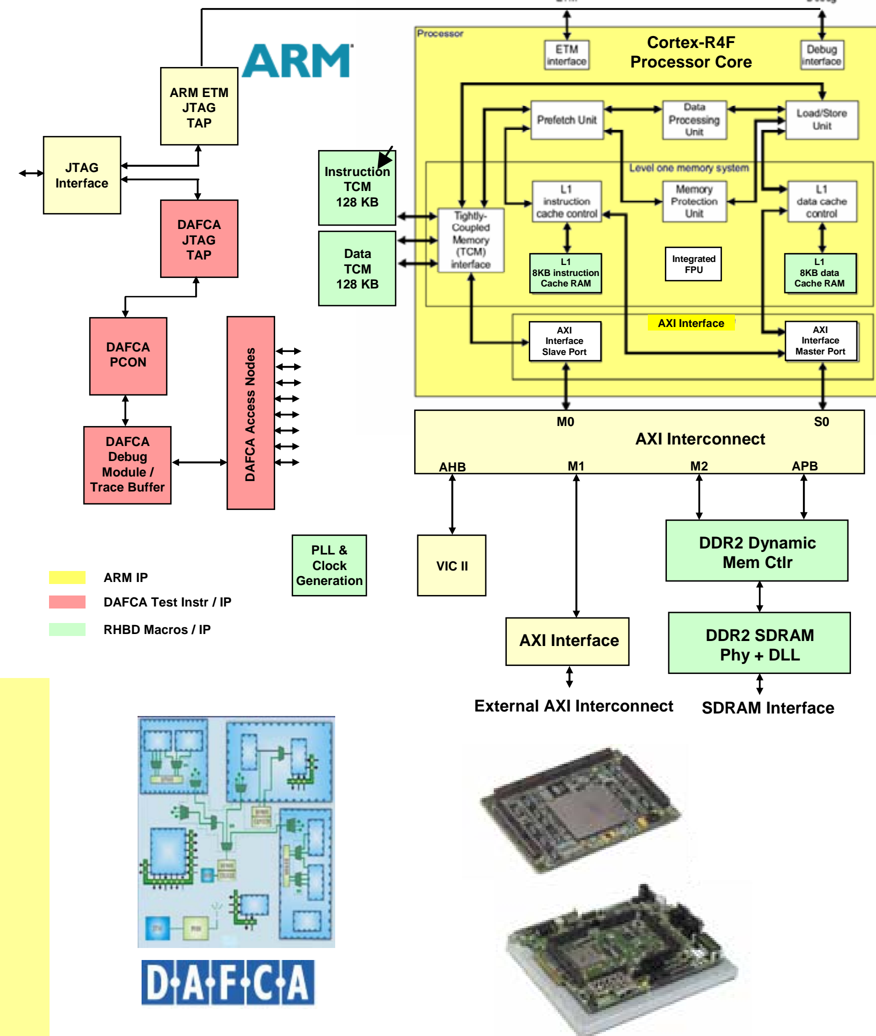
Integration Test Chip & MASETRO

2008				2009				2010			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4

Milestones: MAESTRO Spec., RDR; Design Update; PDR; ITC CDR/Release; ITC Test Comp.; MAESTRO CDR/ Release; MAESTRO Test Comp.; MAESTRO Final Report

PDV2
(Embedded Processing Cores with SEE Instrumentation)

- ARM Cortex with embedded instrumentation
  - Improved observability to SEE subcircuit error rates
  - Observe error propagation from subcircuit to system-level
  - Supports tailored hardening to optimize design
- Use existing commercially available products:
  - Synthesizable processor core and peripherals
  - Testbenches
  - Synthesis-level, at-speed, Design-for-Debug (DAFCA ClearBlue)
  - HW/SW development environment



- Showcases the RHBD technology
- Popular embedded processing cores
- Study SEE-induced errors and their propagation
- Affordable, Low-risk demonstration
- Testable

Master Schedule by Task

	2007	2008				2009			
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4

Design Enablement
- RHBD Library Clock Gen PLL Rad Test Comp.
- Available 3 PDV1 SRAMs
- LVDS, Rad Test Comp.
- SERDES Rad Test Comp.

PDV0
- Packaged Parts
- Tests Completed

PDV1
- PDR
- Release
- Test Complete

PDV2
- Design Start
- RDR
- PDR
- CDR/Release
- Packaged Parts
- Test Comp

Tech. Char.
- V3, SET Parts O/D
- V3, SETP Test Comp
- 65nm TCV1 Release
- 45nm decision
- Next Tech TCV2 Release
- Next Tech TCV2 Evaluation
- SET Mitigation Parts O/D
- SET Mitigation Test Comp
- SET Mitigation Guidelines

Technology Transfer Activities

- The DTRA/Boeing technology development programs, starting in 1996, have had a strong focus on technology transfer.
  - RH Digital Signal Processor
  - Foundry Independent RH Microelectronics
  - RH EDA Very Deep Submicron Microelectronics
  - RH EDA Ultra-Deep Submicron Microelectronics
- Focusing on the RHBD Phase 2 Program technology transfer activities include:
  - Development of this capability at the Boeing "Phantom Works" to serve the entire DOD and commercial satellite and missile system community; N.B. this organization serves as a "pure play" design house with many customers outside of Boeing.
  - Direct transfer to the AF TSAT SPO & Boeing TSAT Program Office WRT Single-Event Effects mitigation at 90nm – In progress and mitigation methods incorporated into Boeing design.
  - Direct support of three OGA Programs; 96 GFLOP DSP and the Opera & Maestro microprocessor architectures – In progress, see PDV-1 discussion.
  - Wide dissemination of the ongoing technology development efforts through briefings at NSREC, HEART, GOMAC, Aerospace Conference and other speaking venues.
  - Significant program review attendance by AF SMC, Aerospace Corp., DARPA, Boeing Space Systems, GD, and others.
- Bottom Line: The government owns this technology and will ensure that it is made available to any and all government contractors and both Boeing and DARPA concur with this position.

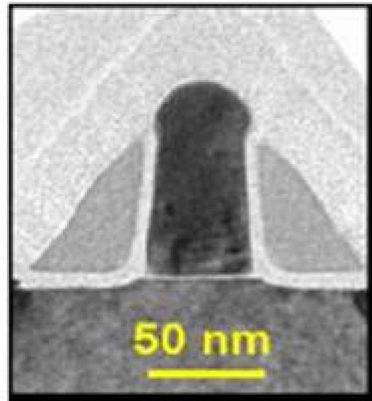
Summary

- RHBD Phase 2 program is on schedule to demonstrate a RHBD 90nm general purpose microprocessor structure identified “Opera” by June 2008
    - Design of Opera previously accomplished through DARPA, USAF & OGA polymorphic computing program)
- RHBD digital 90nm libraries have been demonstrated
- Additional macro-cells to complete the demonstration are in development and on schedule
- The overall program is on schedule (all technical requirements, cost and schedule on track).
- The cell library and macro-cells are owned by the government and available to other government organizations and their contractors

Radiation Hardened Nano-Technology Development Program
(IBM, BAE, HI, CNSE,VU)

< 100nm IBM Commercial Transistor

Starting point for development of RH nano-technology



Objectives

- Develop and demonstrate technology to support the fabrication of < 100nm semiconductor microelectronics
  - Demonstrate radiation hardened 90nm CMOS microelectronics technology
  - Design and develop test structures and circuits to test the efficacy of the hardening approaches
  - Develop radiation effects models

Technical Approach:

- **Investigate 90nm silicon based technologies**
- **Investigate alternative material technologies including molecular materials**
- **Model and simulate radiation responses**

Milestones

- FY06: Two contracts awarded; HI & BAE Systems
- FY07: Investigation of IBM 90nm CMOS technologies initiated
- FY08: Demonstrate 90nm hardened technology
- FY09: Complete technology development and characterization

BAE Systems RH 90nm Program

BAE Systems RH 90nm Program

- Program Description
- Goals and Requirements
- Technical Approach
- Major Accomplishments
  - Testing and Simulation Results
- Technology Transfer
- Summary

Program Description

Program Description: Evaluation of 90nm commercial bulk CMOS technology and initial development of 90nm Rad Hard techniques

Customer: Defense Threat Reduction Agency (DTRA)

Period of Performance: 3/31/06 to 8/31/09

Teammates/Subcontractors: IBM and Vanderbilt University

Collaborators: CNSE, NRL, AFRL, TAPO

Program Objectives:

- Radiation Hardness evaluation of existing 90nm test structures
- Design of Experiments (DOE) of minimally invasive RH techniques
- Design/Fabrication/Evaluation of Technology Characterization Vehicle (TCV)

Goals & Requirements

Table 2.a. - SRAM Requirements and Goals

Parameter	Goal	Requirement
Architecture	64Mbit equivalent	16Mbit equivalent
Operation	N/A	N/A
Operating Voltages (volts)	N/A	N/A
Operating Temperature Range - Full Performance - Functionality	- 55 to 125 °C Same	0 to 80 °C -55 to 125 °C
Operating Speed - worst-case & post irradiation	≤ 5 nsec	≤ 10 nsec
Standby Current - worst-case & post irradiation	≤ 20 ma.	≤ 20 ma
Total Ionizing Dose - (rd(Si)) (4)	≥ 1 M rd(Si)	≥ 500 krd(Si)
Single-Event-Upset - (errors/bit-day) (1)	< 1E-11	< 1E-10
Single-Event-Latchup - (LET in Mev-cm^2/mg) (2)	> 120	> 100
Neutron Irradiation - (Mev eq. n/cm^2)	> 1E13	>1E12
Dose-Rate Upset - (rd(SiO_2)/s) (3)	≥ 1E10	≥ 1E 9
Dose-Rate Survivability - (rd(SiO_2)/s) (3)	1E12	1E12
Failure Rate (Failures in Time - FIT)	N/A	N/A

(1) Adams 10 % Worst-Case environment under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g. static or dynamic operation)
(2) Under worst-case voltage and temperature operating conditions.
(3) Dose-rate testing shall be accomplished using a 20 to 50 nsec FWHM pulse, under worst-case voltage and nominal temperature operating conditions, for both static and dynamic operation. The operation of the device-under-test shall be monitored for memory cell upset, I/O upset defined as a voltage excursion > Vdd/3 and any access time push-out
(4) Testing shall be done IAW MIL-T-1019.5 using a Cobalt-60 source at a dose-rate between 50 to 300 rd(Si)/s

Table 2.b. - ASIC/Gate Array Requirements and Goals

Parameter	Goal	Requirement
Usable Gate Number	≥ 40M equivalent	≥ 20M equivalent
Operating Voltage	N/A	N/A
Operating Speed - worst case & post-irradiation	> 1.5 Ghz	≥ 750 Mhz
Operating Temperature Range - Full Performance - Functionality	- 55 to 125 °C Same	0 to 80 °C 55 to 125 °C
Radiation Requirements (See Table 2a)	Same as SRAM	Same as SRAM
Failure Rate (FIT) (See Table 2a)	Same as SRAM	Same as SRAM

Technical Approach

- Technology evaluation using Road King
- Identify technology capabilities and issues
- Design TCV/CTV and place on TAPO masks
- Short loop development at IBM BTV and ANT
- Radiation TCAD modeling/simulation at VU
- Process integration using TCV/CTV
- Technology validation via electrical and radiation testing of TCV/CTV
- Based on T&E results identify remaining issues for further enhancements

Program Flow Status

2006-2007

RH Nanotechnology
- ✓ Applications & Req. ID
- Capabilities Roadmap
- RH Requirements

2006-2007

Commercial 90nm Technology Evaluation
- ✓ Test Structure Selection/ Fab
- ✓ Radiation Testing*
- ✓ TCAD Model Development

2006-2009

RH 90nm Technology Development
- ✓ Design of Experiments
- ✓ TCV Design
- ➔ Fab/ Radiation Testing
- RH Recommendations

✓ complete
➔ in-process

Major Accomplishments

- Baseline technology radiation testing and characterization completed
- Completed base SEU 3D mixed mode simulations on the 2.3 um^2 memory cell; results shows ample SEU hardness margin with targeted R and C
- Radiation testing on test structures completed
  - Total ionizing dose
  - Single Event Gate Rupture
  - Single Event Upset
- SRAM cell design completed
- TCV designed completed and fabrication initiated

Commercial 90nm Assessment

	Goal	Requirement	Demonstrated Capability
TID	1Mrd	500Krd	<100Krd ✓
SEU	SER<1E-11	SER<1E-10	~1E-6 -1E-7 ✓
SEL	LET>120	LET>100	Epi: LET>120 ✓ Non-Epi: L/U with Protons ✓
PDU	>1E10	>1E9	Epi:>1E10 Static (Short Pulse) ✓ 3E9 Dynamic (Long Pulse) Non-Epi:>2E9 Static (Short Pulse) ✓ >2E8 Dynamic (Long Pulse) L/U: Epi Tested through 2E11 ✓ L/U: Non-Epi ~3E9 ✓
PDS	>1E12	>1E12	Tested through 2E11 with Epi *
Neutron	>1E13	>1E12	Results 2Q2008 *

✓ Demonstrated capability meets requirement

* Expect to meet requirement - not demonstrated yet

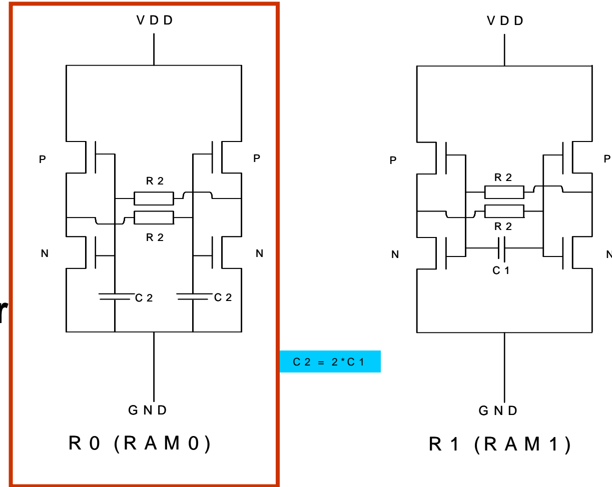
✓ Capability shortfall demonstrated

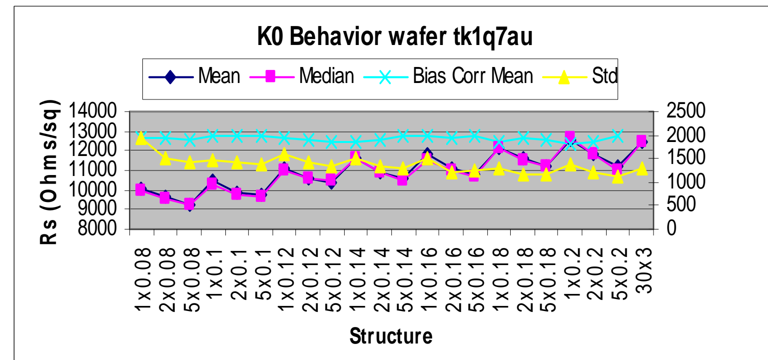
Process Integration Status

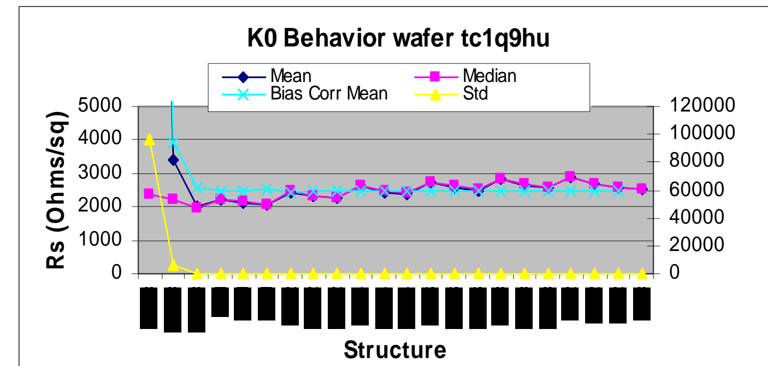
Technology Feature	Integration Status	Potential Tasks
Thin Epitaxial Substrates	Fully Integrated	Optimize Thickness
EG Low Leakage Device	Fully Integrated	Process Centering
Enhanced STI	Integration Hardware in Progress	Verify Parameters and TID Sidewall Implant Optimization
Deep Trench Capacitor	Fully Integrated	Optimize Value – Deeper Trench
K0 Resistor Integration	Fully Integrated	Validation on SRAM
Fully Integrated RH90	First Pass Fully Integrated	Process Optimization Larger Data Base
Yield and Producibility	Limited Demonstration	Shrunk 16M SRAM
Technology Applications	Limited Circuit Demonstration	CTV Phase

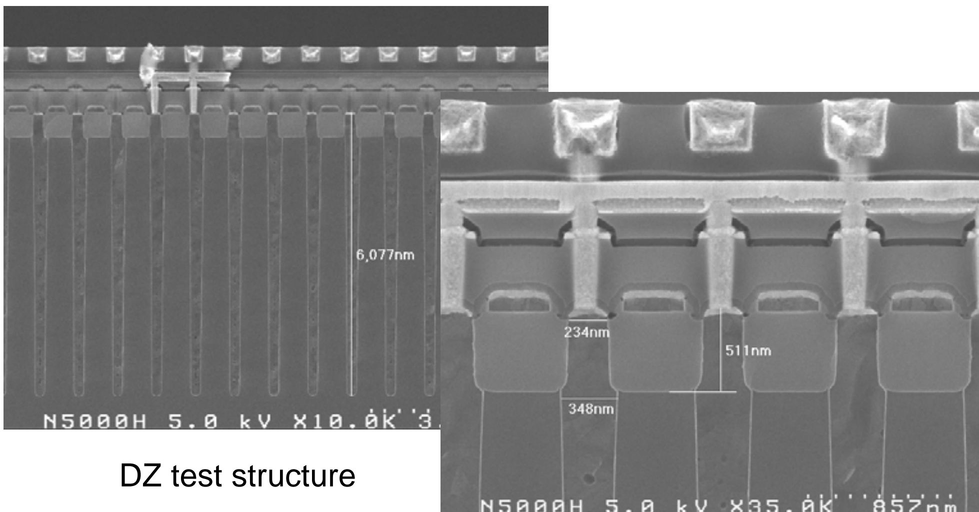
Robust Trench Capacitor & Resistor Key to SEE Mitigation

- **Capacitance Measured**
  - **~ 17.8 fF / trench**
  - **Earlier RoadKing (RK) work was 23 fF (1V)**
  - **Currently 4-5x higher than possible with advanced MIM**









DZ test structure

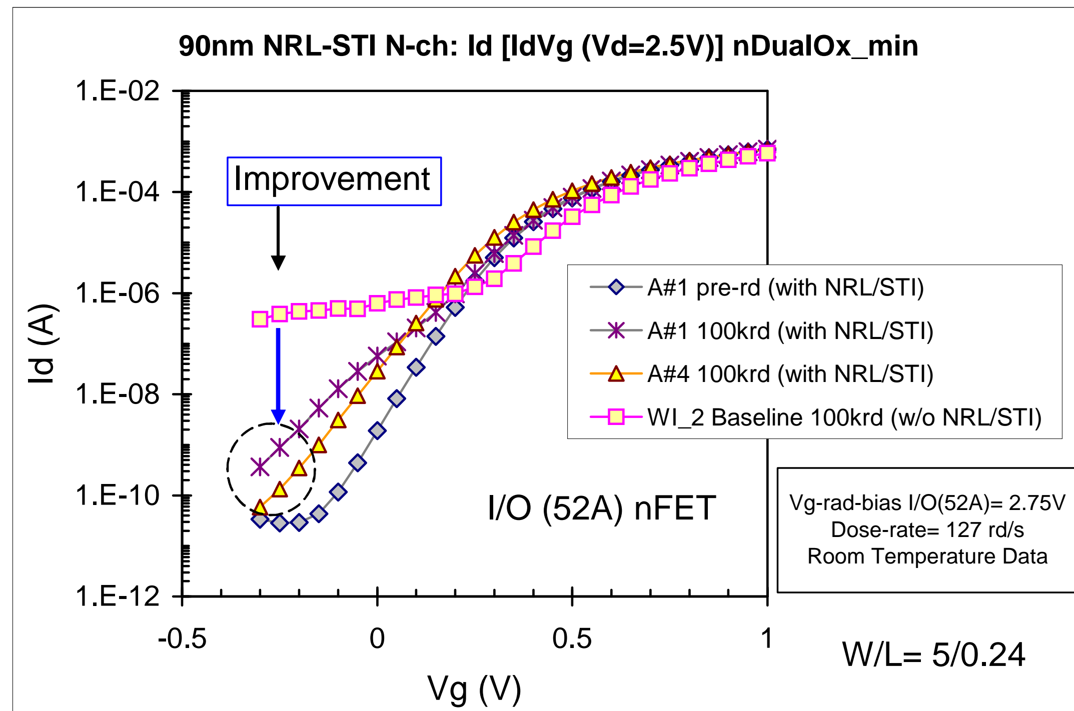
DZ to Pwell leakage ~ 2 fA/trench

TID on 9SF NRL Modified STI transistors

- TID Cobalt-60 (1 MeV gamma-ray) testing on IBM 9SF LSM 90nm field effect transistors (FETs) from Road-King Prime A
  - Test structures had a modified shallow trench isolation (STI) fill as defined by the Naval Research Laboratory (NRL)
  - The TID testing was done on 2 packages which contained a total of 8 transistor structures

Key TID Observations

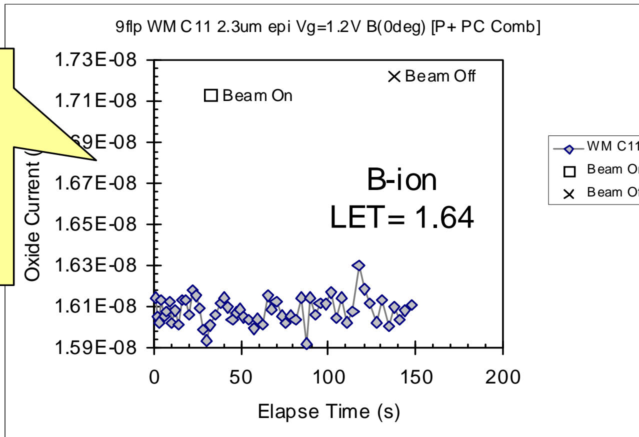
- N-channel input/output (I/O) FETs showed reduced TID induced edge leakage with the NRL-STI process
- N-channel core FETs showed almost no TID induced degradation. This result was observed with or without the NRL-STI process.

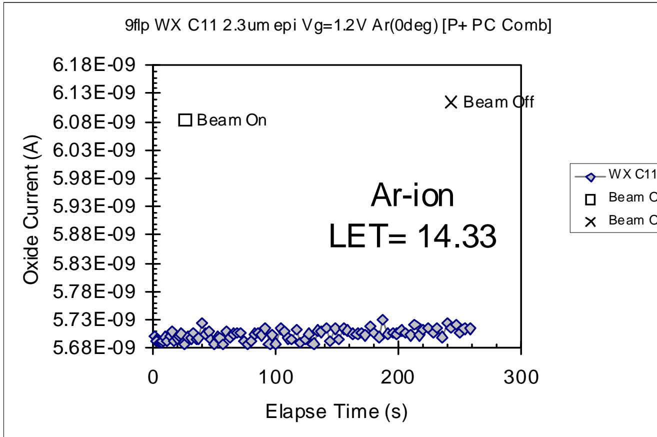


9FLP SEGR Test Results

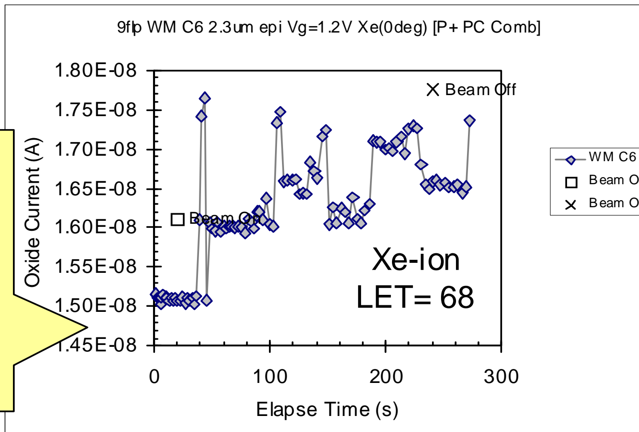
Typical 9FLP SEGR dataset (Vg= 1.2V shown, Fluence(max)= 2E8 ions/cm^2)

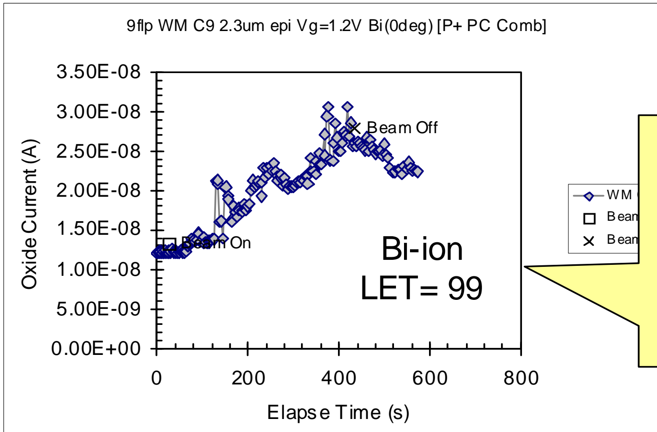
For lower LET values, no observed change





For higher LET values, begin to see small data jumps





For Max LET value, data shows continuous increase

No powers-of-10 increase in gate-oxide current detected [No SEGR events]

Technology Characterization Vehicle

TCV Overview

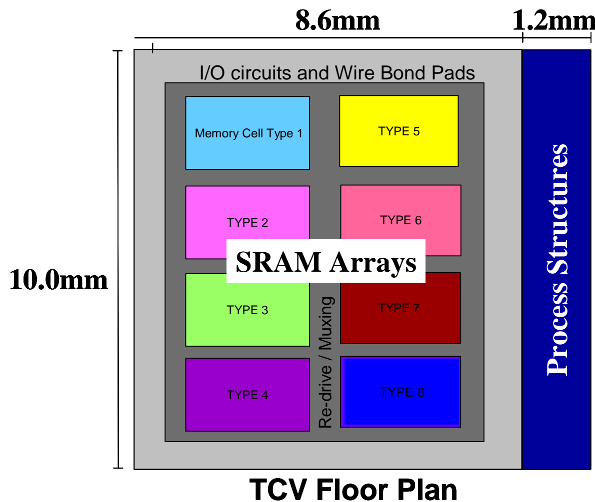
- Transistors
  - 14A, 22A and 52A
  - Std, Regular and High Vt
- SRAMs
  - Six designs
  - Commercial to Aggressive

FETs

90nm (9SF) Transistor	Description	Gate Oxide	Channel Length	Operating Voltage
SG	Single Gate Standard 9SF	14A	0.08µm	1.0V/1.2V
EGV	Regular Vt HS/IO - Lower Voltage	22A	0.10µm	1.2V
HEGV*	High Vt HS/IO - Lower Voltage	22A	0.10µm	1.2V
EG	Regular Vt HS/IO - Higher Voltage	22A	0.12µm	1.5V
HEG*	High Vt HS/IO - Higher Voltage	22A	0.12µm	1.5V
DGV	Regular Vt IO - Lower Voltage	52A	0.20µm	1.8V
DG	Regular Vt IO - Higher Voltage	52A	0.24µm	2.5V

** New devices; not part of 9SF commercial offering*

Tests= TID



TCV Floor Plan

SRAMs

SRAM Type	Memory cell / area	Core gate oxide	Vt	Operating Voltage	Resistor / Value	Trench Cap / value
1. Commercial like array - 14A	6T / 2.55um^2	14A	Regular	1.0V / 1.2V	no	no
2. Commercial like array - 22A	6T / 2.55um^2	22A	Regular	1.2V	no	no
3. Commercial like array - 22A High Vt	6T / 2.55um^2	22A	High Vt	1.2V	no	no
4. Aggressive cell w/ trench	6T2R2C / 2.34 um^2	22A	High Vt	1.2V	90K?	25fF
5. Conservative cell w/ trench (Low R)	6T2R2C / 4.41 um^2	22A	High Vt	1.2V	50K?	25fF
6. Conservative cell w/ trench (High R)	6T2R2C / 4.41 um^2	22A	High Vt	1.2V	140K?	25fF

Tests= TID, SEE (HI & proton)

RH 90nm Development Radiation Test Program

Baseline 2007

- Commercial 90nm Technology (SRAM built on epitaxial silicon)
  - TID (30krd to 300krd)
  - SEU (SER 3E-7 u/b-d)
  - SEGR (oxide degradation)
  - Latch-Up (LET= 100; Vdd +10%)
  - Prompt Dose (>1E9 rd/s)

Technology Characterization Vehicle (TCV) 2008

- Enhanced 90nm Technology
  - TID
    - Modified STI
  - SEU and Latchup
    - Layout and design
  - SEGR
    - Trench Capacitor

RH90 Technical Outlook

Table 2.a. - SRAM Requirements and Goals

Parameter	Goal	Requirement
Architecture	64Mbit equivalent *	16Mbit equivalent *
Operation	N/A	N/A
Operating Voltages (volts)	N/A	N/A
Operating Temperature Range - Full Performance - Functionality	- 55 to 125 °C Same	0 to 80 °C -55 to 125 °C
Operating Speed - worst-case & post irradiation	≤ 5 nsec *	≤ 10 nsec *
Standby Current - worst-case & post irradiation	≤ 20 ma. *	≤ 20 ma *
Total Ionizing Dose - (rd(Si)) (4)	≥ 1 M rd(Si) *	≥ 500 krd(Si) *
Single-Event-Upset - (errors/bit-day) (1)	< 1E-11 *	< 1E-10 *
Single-Event-Latchup - (LET in Mev-cm^2/mg) (2)	> 120 *	> 100 *
Neutron Irradiation - (Mev eq. n/cm^2)	> 1E13 *	>1E12 *
Dose-Rate Upset - (rd(SiO_2)/s) (3)	≥ 1E10 *	≥ 1E 9 *
Dose-Rate Survivability - (rd(SiO_2)/s) (3)	1E12 *	1E12 *
Failure Rate (Failures in Time - FIT)	N/A	N/A

(1) Adams 10 % Worst-Case environment under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g. static or dynamic operation)
(2) Under worst-case voltage and temperature operating conditions.
(3) Dose-rate testing shall be accomplished using a 20 to 50 nsec FWHM pulse, under worst-case voltage and nominal temperature operating conditions, for both static and dynamic operation. The operation of the device-under-test shall be monitored for memory cell upset, I/O upset defined as a voltage excursion > Vdd/3 and any access time push-out
(4) Testing shall be done IAW MIL-T-1019.5 using a Cobalt-60 source at a dose-rate between 50 to 300 rd(Si)/s

Table 2.b. - ASIC/Gate Array Requirements and Goals

Parameter	Goal	Requirement
Usable Gate Number	≥ 40M equivalent *	≥ 20M equivalent *
Operating Voltage	N/A	N/A
Operating Speed - worst case & post-irradiation	> 1.5 Ghz *	≥ 750 Mhz *
Operating Temperature Range - Full Performance - Functionality	- 55 to 125 °C Same	0 to 80 °C 55 to 125 °C
Radiation Requirements (See Table 2a)	Same as SRAM	Same as SRAM
Failure Rate (FIT) (See Table 2a)	Same as SRAM	Same as SRAM

- Technical activities on schedule to meet all requirements and most of the goals
- Degrees of challenge:

Low * **Medium** * **High** *

Summary

- Program on schedule
- Radiation testing validated radiation sensitivity of commercial 90nm
- Design of experiments (DOE) short loops complete
- TCV integration lots complete
- Fully integrated TCV lots in progress
- TCAD simulation complete; to be verified by hardware test

Honeywell RH 90nm Program

Honeywell SSED RH 90nm Program

- Program Objectives
- Major Accomplishments
- Technology Development Status
- Schedule
- Summary

Program Objectives

- Objectives of the program
  - Design, fabricate, test and evaluate nanotechnology test structures and circuits to support radiation testing and characterization
  - Characterize and project the radiation response of those identified technologies
  - Develop radiation hardening technology suitable to support the demonstration of RH nanotechnology devices and circuits

Honeywell / IBM Collaboration

- Honeywell has teamed with IBM to develop a 90nm rad-hard SOI technology
- Based on IBM's 90nm SOI technology, with Honeywell's radiation hardening technology added
  - Multiple Vt's, single core gate oxide, 63nm Lpoly, body tied
  - 10LM
  - Low k Copper BEOL
  - Deep trench capacitor and IP
  - TaN resistor
- First phase will demonstrate all key modules necessary to achieve the desired SRAM cell size and have the devices needed for SER hardening

Requirements/Goals

Table 2. - Technology Goals and Requirements

Parameter	Goal	Requirement
Architecture		
SRAM Cell Size	$\leq$ 1.25 microns-sq	$\leq$2.5 microns-sq
Density (Kgates per mm-sq)	400	250
Operating & I/O Voltages (volts)	1.0, 1,2, 2.5 and 3.3 volts	1.0, 1.2 and 2.5 volts
Operating Temperature Range - Full Performance - Functionality	- 55 to 125 ^{o}C Same	0 to 80 ^{o}C -55 to 125 ^{o}C
Operating Speed - worst-case & post irradiation	$\leq$ 10ps delay for an unloaded Ring Oscillator (RO)	$\leq$ 20 psec for an unloaded RO
Standby Current - worst-case & post irradiation per 10Mgates	$\leq$ 100 ma.	$\leq$500 ma
Total Ionizing Dose - (rad(Si)) (5)	$\geq$ 1 M rd(Si)	$\geq$ 500 krd(Si)
Single-Event-Upset - (errors/bit-day) (1)	< 1E-12	< 1E-10
Single-Event-Latchup - (LET in Mev-cm^2/mg) (2)	> 120	> 100
Neutron Irradiation - (1 Mev equiv. n/cm^2)	> 1E13	>1E12
Dose-Rate Upset - (rad(Si)/s) (3)	$\geq$ 1E11	$\geq$ 1E 9
Dose-Rate Survivability - (rad(Si)/s) (4)	1E12	1E12
Failure Rate (Failures in Time - FIT)	N/A	N/A

(1) Adams 10 % Worst-Case environment under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g. static or dynamic operation)
(2) Under worst-case voltage and temperature operating conditions.
(3) Dose-rate testing shall be accomplished using a 20 to 50 nsec FWHM pulse, under worst-case voltage and nominal temperature operating conditions, for both static and dynamic operation. The operation of the device-under-test shall be monitored for memory cell upset, I/O upset (defined as a voltage excursion > Vdd/3) and any access time push-out.
(4) Dose-rate testing shall be accomplished using a 20 to 50 nsec FWHM pulse, under worst-case voltage and nominal temperature operating conditions for static operation.
(5) Testing shall be done IAW MIL-T-1019.5 using a Cobalt-60 source at a dose-rate between 50 to 300 rd(Si)/s.

Process Development Status

Building Blocks	Requirement	Experience / Plan
Transistor Design	**VT = 500mV** **Parameters to meet revised SOW**	Targets Hit on GQRH lot2. Investigation of 2nm gate ox/ 63nm Lpoly on GQRH3 for common ASIC and SRAM technology.
Body Tie	**Si thickness = 25nm** **Fox coverage > 30nm** **R < 10Kohm/sq**	Shortloop wafers and GQRH lots have demonstrated physical targets on 4 passes. First pass success with HI body tie integrated with IBM SOI process, GQRH lot2. Nbody tie resistance met target and Pbody tie R within tunable range, (high by ~40%), implant dose adjustment to be verified on GQRH3.
Capacitor	**40-60 fF per unit cap** **Leakage <5 pA/cap DTcap on SOI**	Shortloop demonstration of trench etch, buried plate doping, capacitor dielectric, poly fill, and recess. Further shortloops planned for assessing nitride protection of SOI top Si and further refinement.
Resistor	**Rs = 10Kohm/sq** **Rs stable with process** **Acceptable TCR**	Stable film demonstrated up to 10Kohm/sq on shortloop wafers. Contacts verified to top and bottom of resistor film. Currently assessing film TCR. Simulations in progress to define TCR requirement
SRAM cell size	**<2.5um²**	3 Key enablers Identified - Direct body tie contact (shortloop start planned for April) - Direct resistor contact (demonstrated) - N SOI substrate (shortloop start planned for April)

RH Enabling Technology Development Projects

Enabling Technology Development Project Contributors

- ASU
- CFDRC
- Lynguent
- MRDC
- Orora
- RAD
- Robust Chip, Inc.
- Vanderbilt University

RH 90nm Technology Development and Demonstration Program Summary

- The DTRA RHM Program is pursuing the development and demonstration of RH 90nm technology through two basic approaches:
  - A Joint RHBD project with DARPA with Boeing/IBM
  - Two RHBP technology development efforts with BAE/IBM and Honeywell/IBM
- RHBD project is on schedule to test and characterize two PDV devices by 4QCY2009 .
- RHBP efforts are scheduled to demonstrate an integrated RH 90nm process by 2009
  - Follow-on program required to demonstrate a RHBP PDV.
- In addition, a number of enabling technology projects are underway to address specific issues such as SEE and radiation response modeling and characterization.