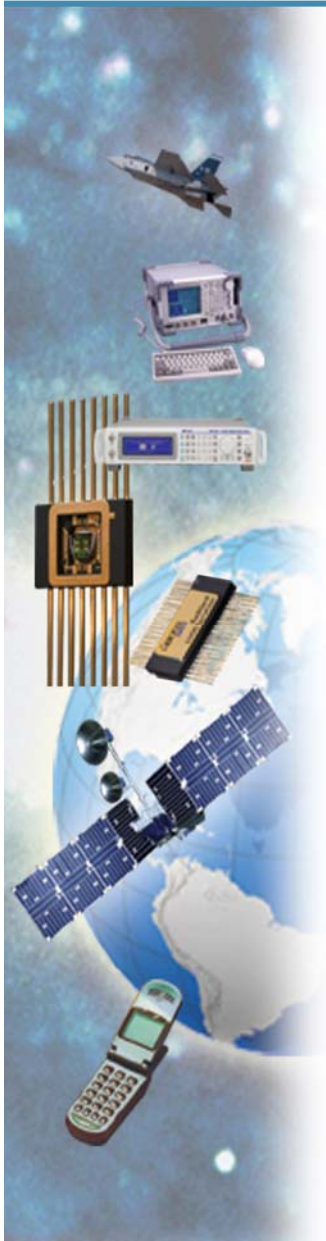


# UT699 32-bit Fault-Tolerant LEON 3FT/SPARC™ V8 Processor

Aeroflex Colorado Springs  
800-645-8862  
[www.aeroflex.com/LEON](http://www.aeroflex.com/LEON)

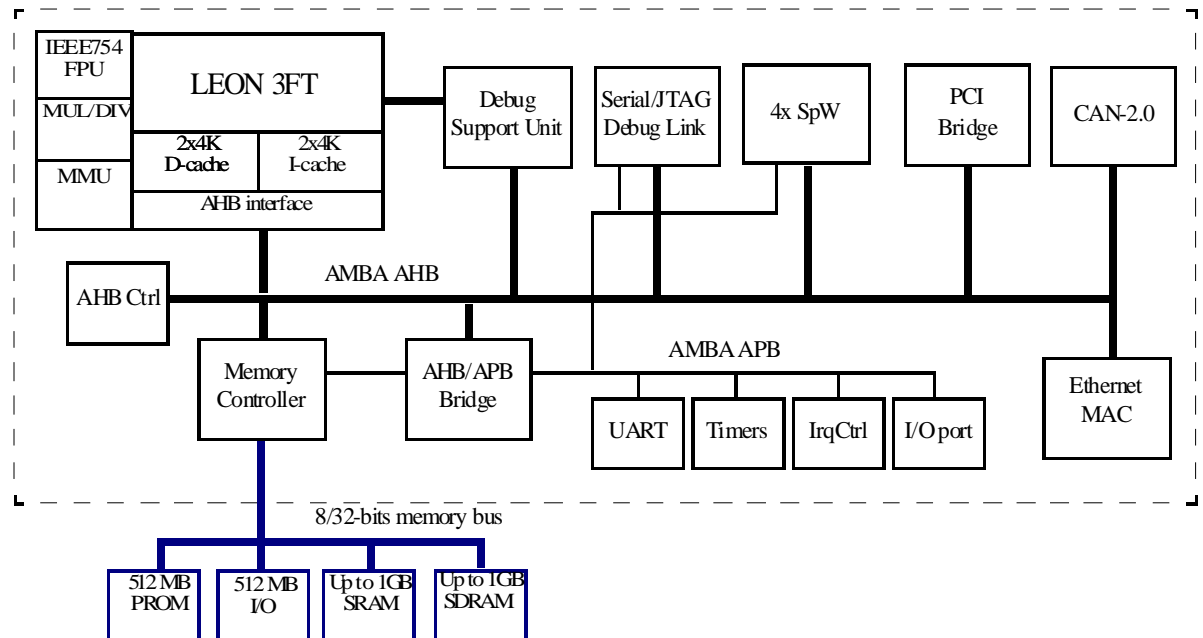
April 2009



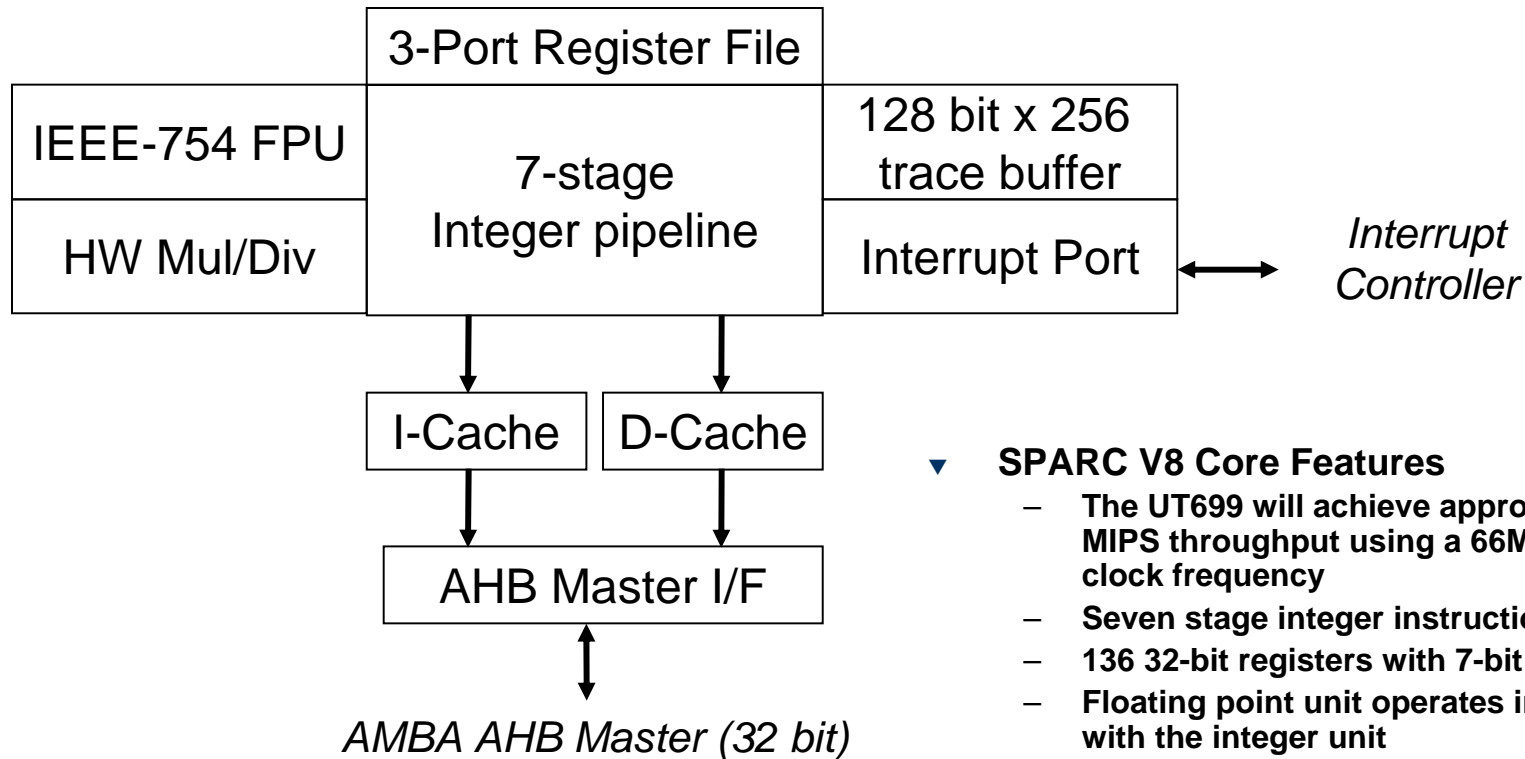
# UT699 LEON 3FT Description



- ▼ Operates from 3.3V for I/O and 2.5V for core
- ▼ Memory controller supports PROM, SRAM, SDRAM, and I/O
- ▼ Debug support unit with trace buffer
- ▼ 4 SpaceWire ports with a data signaling rate to 200 Mbits/s full duplex mode
- ▼ 32-bit / 33 MHz PCI port
- ▼ 2 CAN 2.0 ports
- ▼ 10/100 Ethernet port
- ▼ Extended Temperature Levels (-40°C to 105°C)
- ▼ Total Dose 300 krads(Si)
- ▼ 352-pin Ceramic Quad Flatpack or 484-pin Land Grid Array
- ▼ QML Q & V Pending



# UT699 LEON 3FT SPARC V8 Core



## ▼ SPARC V8 Core Features

- The UT699 will achieve approximately 53 MIPS throughput using a 66MHz base clock frequency
- Seven stage integer instruction pipeline
- 136 32-bit registers with 7-bit checksum
- Floating point unit operates in parallel with the integer unit
- 2x4k data and 2x4k instruction cache in a two-way set associative configuration
- 32 byte per line instruction cache and 16 byte per line data cache
- Cache RAMs use 4-bit parity / force cache miss on error

## ▼ Internal Registers

- Comprised of the Integer Unit (IU), Floating Point Unit (FPU), and configuration registers
- IU register file uses 7-bit checksum for SEU protection
- IU status registers include the Program Counter (PC) and Processor State Register (PSR)
- Register file comprised of the  $r$  registers can be used as operand registers
- Status registers can be read from and written to using the READ and WRITE commands with the  $r$  registers, e.g. to read the Program Counter register into register  $r[24]$ :

```
rd %pc, %r24
```

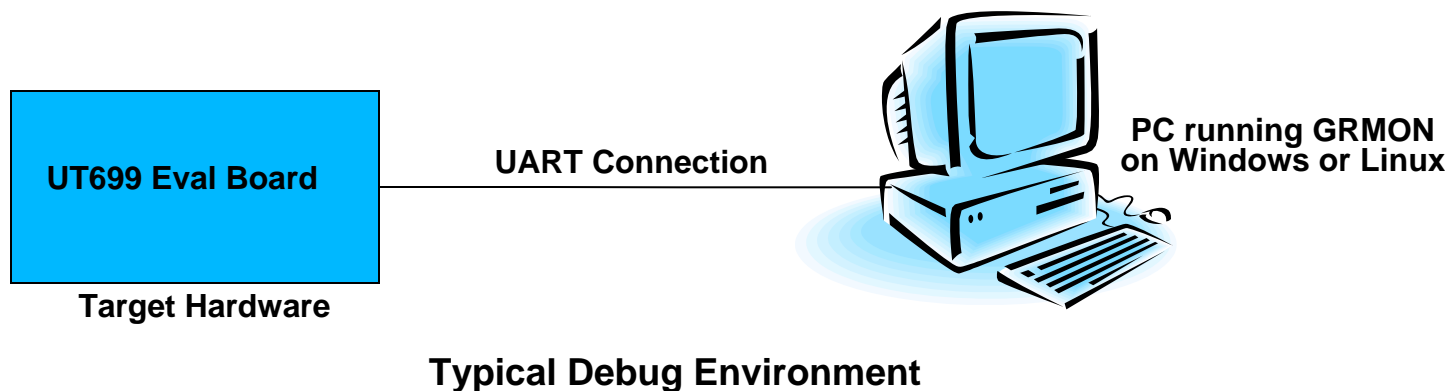
r[31]
r[30]
...
...
...
...
...
r[2]
r[1]
r[0]

$r$  registers

# UT699 LEON 3FT

## ▼ On-chip debug support (DSU)

- The DSU provides non-intrusive debugging on target hardware
- The DSU can be accessed via a dedicated UART, JTAG port, a SpaceWire port, or through the PCI interface
- The DSU also allows single stepping, instruction tracing and hardware breakpoint/watchpoint control
- Full access to all processor registers and cache memory is provided
- A 128-bit x 256 line internal trace buffer can monitor and store executed instructions



## ▼ AMBA Interface

- The Advanced Microcontroller Bus Architecture (AMBA) interface is a 32-bit bus compliant with the AMBA-2.0 standard and operates at the system clock frequency
- The AMBA bus is comprised of the high speed AHB bus used for data transfer, and the APB bus for low speed access to the configuration registers
- Cache loads and stores occur over the AHB bus
- Peripherals transfer data over the AHB bus via FIFO registers
- Incremental bursts are generated to optimize the data transfer during cache line refill

## ▼ Power-down/Standby Mode

- Power-down mode halts the pipeline and caches until the next interrupt and is entered with the following command

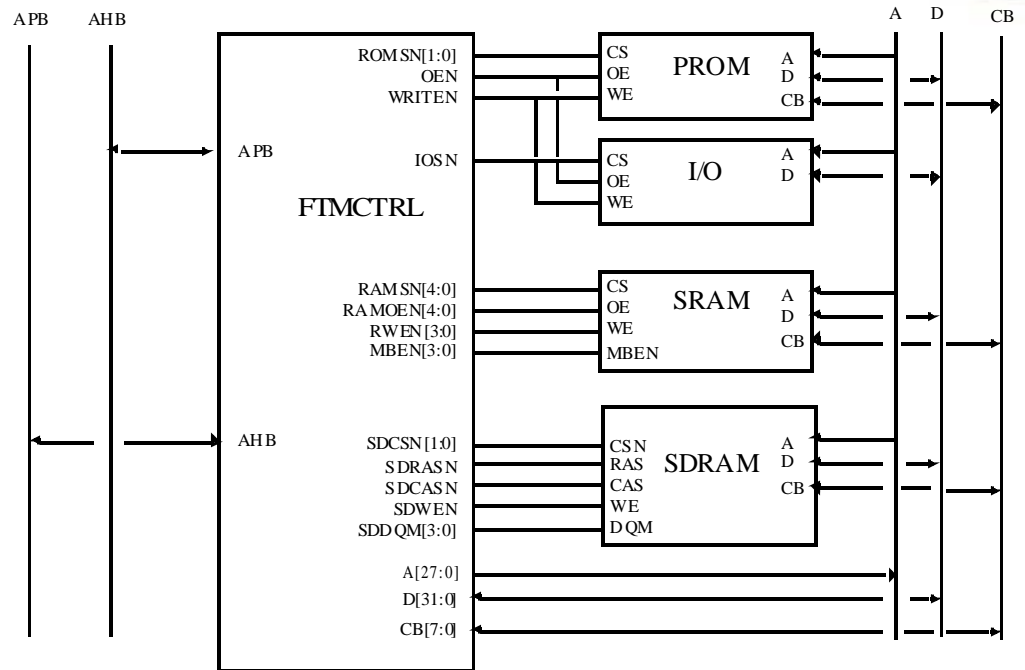
```
wr %g0, %asr19
```

- Each peripheral can be shut off via a register write
- Typical power down current less than 180mA core and 50uA I/O
- Worst case quiescent current less than 20mA core and 750uA I/O

# UT699 LEON 3FT Memory Controller



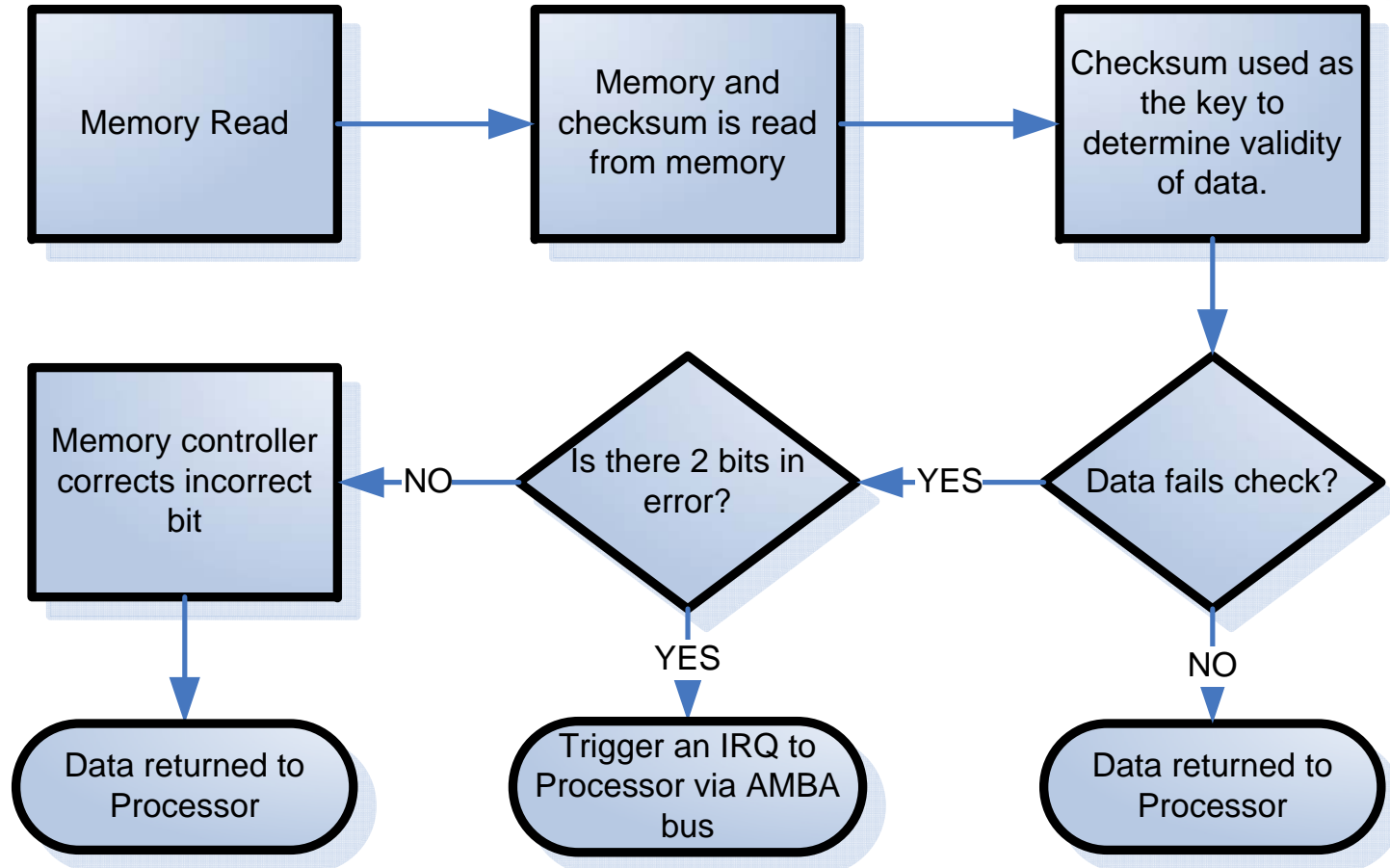
- **Memory Interface Error Correction:**
  - The PROM, SRAM and SDRAM areas are EDAC protected using a (39, 7) block Hamming code
  - The EDAC uses 7 check bits CB[6:0]
  - The EDAC provides single-error correction and double-error detection for each 32-bit memory word
- The memory controller provides independent control over the following interfaces
  - 256 MB addressable space for PROM
  - 512MB addressable space for I/O
  - 1GB addressable space shared between SRAM and SDRAM



FTMCTRL	0x00000000 – 0x1FFFFFFF : PROM area 0x20000000 – 0x3FFFFFFF : I/O Area 0x40000000 – 0x7FFFFFFF : SRAM/SDRAM area	AHB
FTMCTRL	0x80000000 – 0x800000FF : Registers	APB

Memory Controller Registers

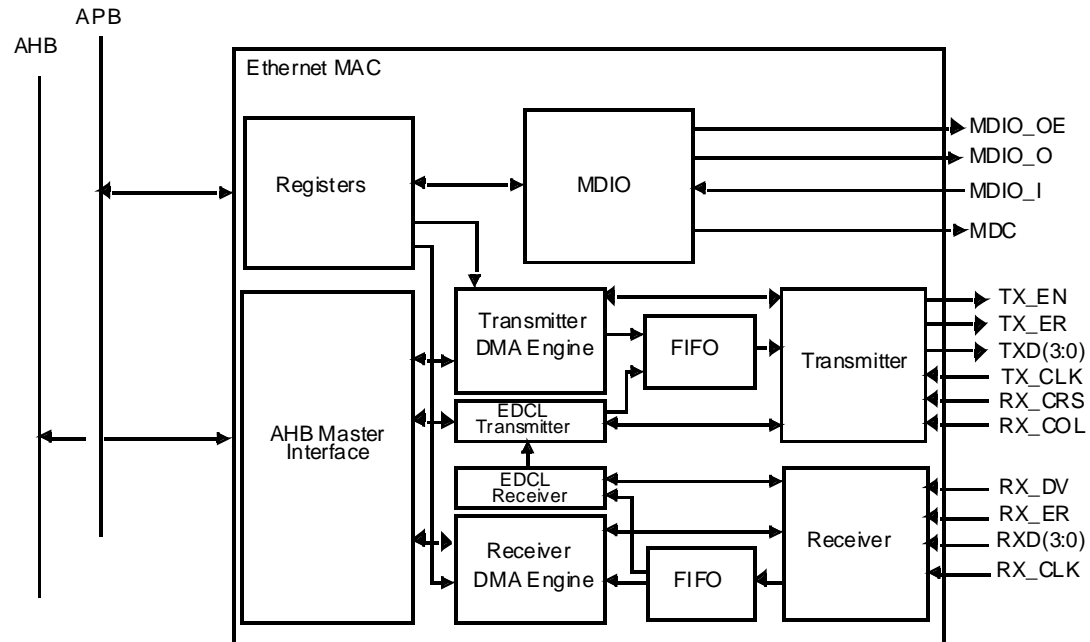
# EDAC Memory Error Detection



# UT699 LEON 3FT Ethernet Controller



- **Ethernet Interface**
  - Ethernet Media Access Controller (MAC) provides a Media Independent Interface (MII) and a Reduced Media Independent Interface (RMII) between the AMBA AHB bus and the Ethernet network PHY
  - Supports 10/100 Mbit speed in both full- and half-duplex
  - Dataflow is handled through DMA channels.
  - One DMA engine for the transmitter and one for the receiver
  - Requires an external 33 MHz clock connected to the RX\_CLK and TX\_CLK inputs



ETH	0x80000E00 - 0x80000EFF : Registers	APB
-----	-------------------------------------	-----

Ethernet Controller Registers

# UT699 LEON 3FT General Purpose Timer



- **Timer Operation**
  - The timer unit acts a slave on AMBA APB bus implementing one 16-bit pre-scale and 4 decrementing 32 bit timers
  - The unit can be configured to issue an interrupt based on several counter conditions as well as individual count set points
  - Uses the internal system clock as the clock source



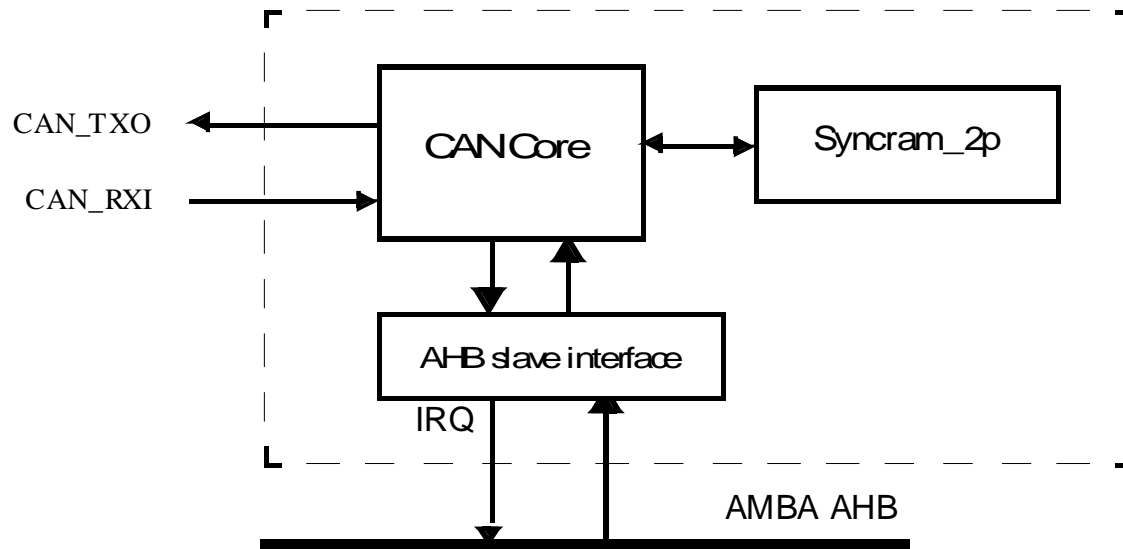
GPTIMER	0x80000300-0x80003FF: Registers	APB
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Timer Controller Registers

# UT699 LEON 3FT CAN I/F



- **CAN Bus Operation**
  - The CAN interface implements the CAN 2.0A and 2.0B protocols. It is based on an industry standard CAN controller utilizing a similar register map
  - Uses the internal system clock as the clock source



CANOC1	0xFFFF20000 – 0xFFFF200FF : Registers	AHB
CANOC2	0xFFFF20100 – 0xFFFF201FF : Registers	AHB

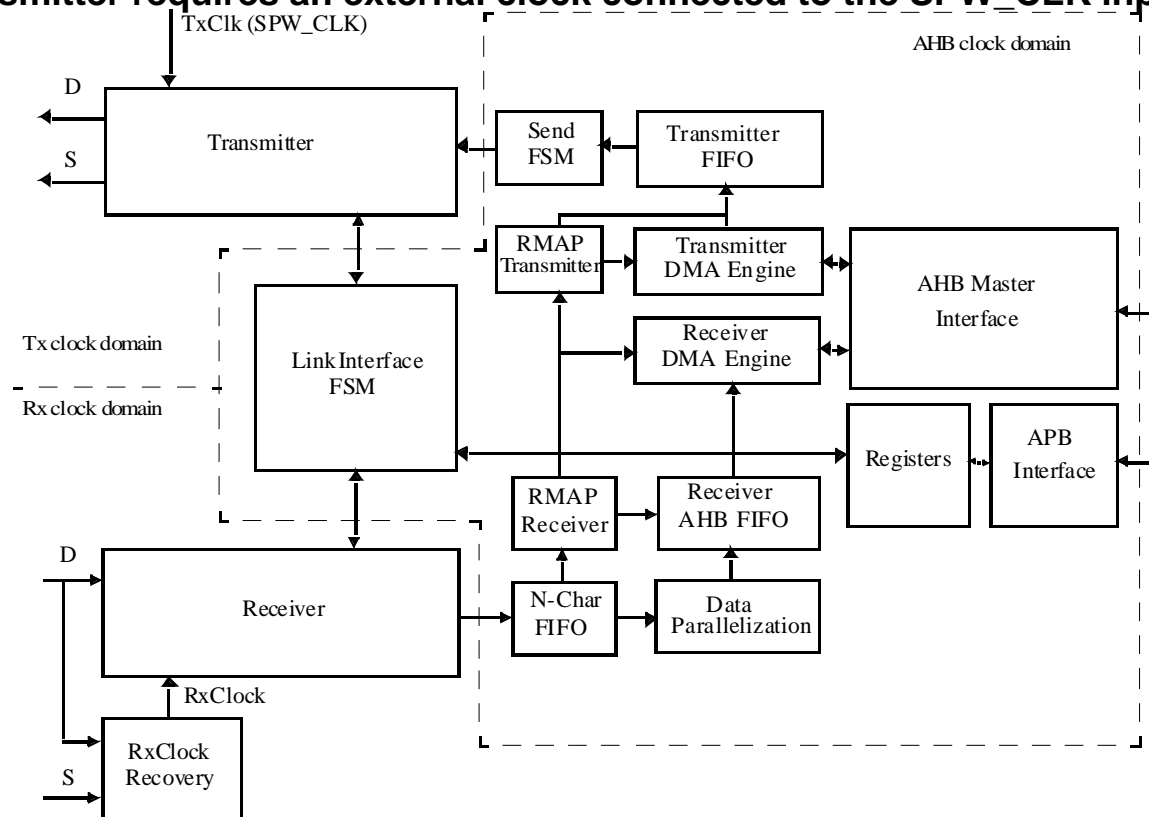
CAN Controller Registers

# UT699 LEON 3FT SpaceWire I/F



## ◆ Space Wire Operation

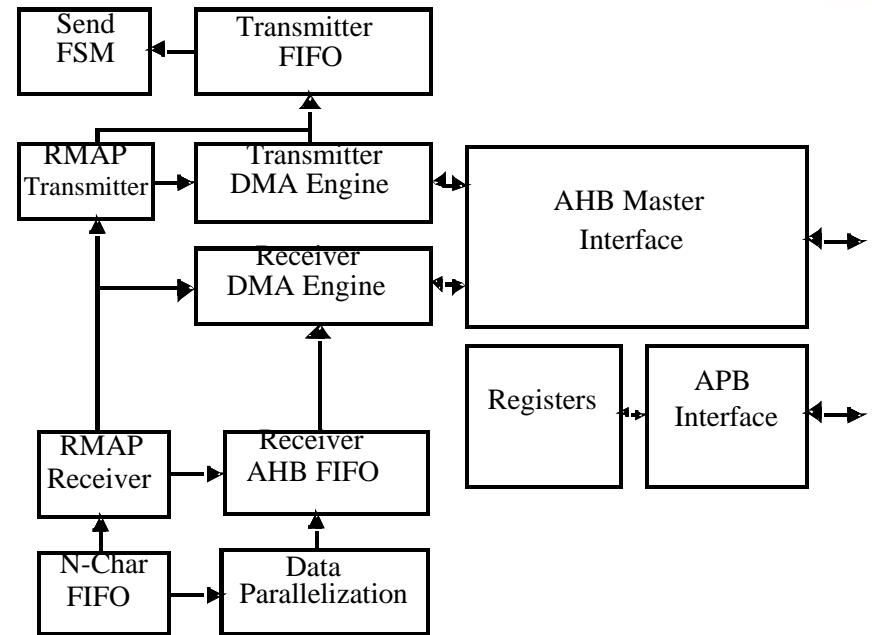
- The SpaceWire interface is comprised of three main parts: the link interface, the AMBA interface and the RMAP handler
- The link interface consists of the receiver, transmitter and the link interface FSM (finite state machine). They handle communication on the SpaceWire network
- The current architecture will support data signaling rates up to 200Mbit/s on all 4 transmit/receive SpaceWire ports in full duplex mode
- The transmitter requires an external clock connected to the SPW\_CLK input



# UT699 LEON 3FT SpaceWire I/F



- **AMBA Bus Interface/RMAP Handler**
  - The AMBA interface consists of the DMA engines, the AHB master interface and the APB interface
  - The RMAP handler is an optional function that can be enabled on nodes 3 and 4
  - When enabled, the RMAP handler handles incoming packets which are determined to be RMAP commands instead of the receiver DMA engine
  - Once the RMAP command is decoded and validated, the read/write operation is performed on the AHB bus
  - Command replies are automatically transmitted back to the source by the RMAP transmitter



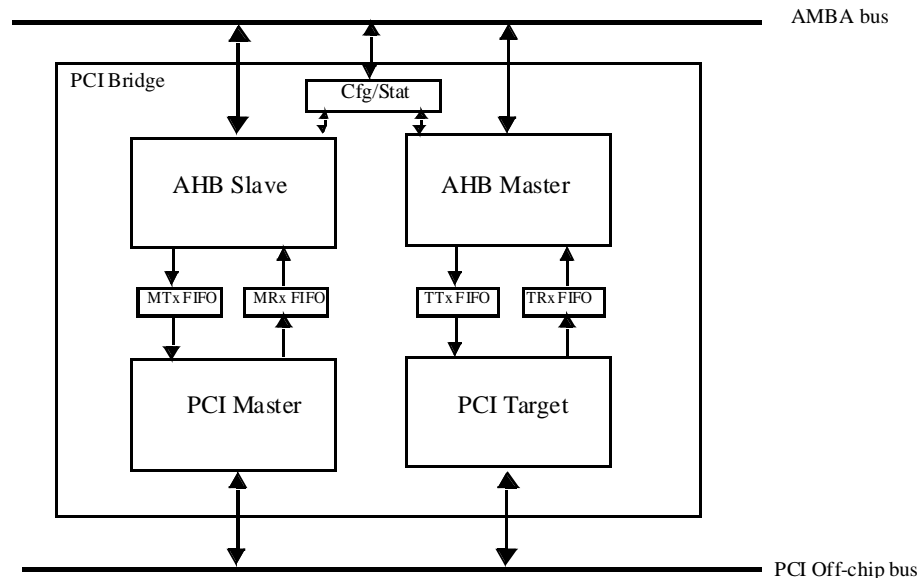
SPW1	0x8000A00 – 0x8000AFF : Registers	APB
SPW2	0x8000B00 – 0x8000BFF : Registers	APB
SPW3	0x8000C00 – 0x8000CFF : Registers	APB
SPW4	0x8000D00 – 0x8000DFF : Registers	APB

SpaceWire Controller Registers

# UT699 LEON 3FT PCI Interface



- **PCI Master/Target Interface**
  - The PCI Target/Master Unit is connected to the PCI bus through two interfaces: the PCI Target and PCI Master
  - The PCI and AMBA interfaces belong to two different clock domains (33MHz and AMBA Clock) with synchronization performed via FIFO registers
  - The PCI Target/Master is capable of handling configuration as well as single or burst memory cycles on the PCI bus
  - Each PCI Target/Master interface is mapped to a 256MB block of AHB memory address and a 128 KB AHB IO address space
  - The Target/Master interface is mapped to external memory via the BAR0 and BAR1 registers



PCI	0x80000400 – 0x800004FF : PCI DMA control registers	APB
PCIARB	0x80000800 – 0x800008FF : Registers	APB

PCI Controller Registers

# Aeroflex UT699 LEON 3FT $\mu$ PROCESSOR

## Software Support Fact Sheet

(C Cross Compiler and Device Drivers provided with Eval Board)



DEVELOPMENT TOOL	SOFTWARE PACKAGE	DOWNLOAD STATUS	WEB	SUPPORTED PLATFORMS	DETAILS
Real Time Operating System	WindRiver VxWorks Version 6.5	Requires license	<a href="http://www.windriver.com">www.windriver.com</a>	Sun Solaris Windows NT/2000/XP	High performance, scalable kernel with small footprint.
	Snapgear embedded Linux for LEON Version 4.6.5	Free	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows (Cygwin)	Contains kernel, libraries and application code for rapid development of embedded Linux applications
	RTEMS-4.6.5 C/C++ real-time kernel Version 4.6.5	Free	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows NT/200/XP	Multitasking capabilities; supports multiprocessor systems, priority based and pre-emptive scheduling
	eCOS real time operating system	Free with License	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows NT/2000XP	Flexible, configurable, real time embedded kernel
C Compiler	Bare-Cross Compiler (BCC) GCC C/C++ (v.3.4.4)	Free	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows	Based on GNU compiler tools and Newlib standalone C library to compile eCos kernel
	RTEMS Cross-Compiler (RCC) GCC-3.2.3 CC++	Free	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows	RTEMS-4.6.5 C/C++ real-time kernel with LEON 3FT support and BSP.
	Eclipse C/C++ IDE	Free	<a href="http://www.gaisler.com">www.gaisler.com</a>	Linux Windows	Integrated development environment for BCC and RTEMS
Debugger	GRMON	Requires License	<a href="http://www.gaisler.com">www.gaisler.com</a>	Sun Solaris, Linux, Windows	Debug monitor. Communicates with LEON debug support (DSU)
Simulator	TSIM GRSIM	Requires license	<a href="http://www.gaisler.com">www.gaisler.com</a>	Sun Solaris, Linux Windows 2000/XP	Standalone or connection to GNU debugger. GRSIM supports multiprocessor systems
Board Support Package	WindRiver VxWorks Version 6.5 – LEON	Requires License	<a href="http://www.gaisler.com">www.gaisler.com</a>	Windows, Linux	LEON driver support for VxWorks 6.5

# Aeroflex UT699 LEON 3FT $\mu$ PROCESSOR

## Industry Comparison



	<b>UT699 LEON 3FT <math>\mu</math>Processor</b>	<b>AT697E</b>	<b>TSC695F</b>	<b>TSC695FL</b>	<b>LEON 3FT RTAX IC</b>	<b>LEON 3FT RTAX SC1</b>	<b>LEON 3FT RTAX SC2</b>
Architecture	SPARC V8 LEON 3FT	SPARC V8 LEON 2FT	SPARC V7	SPARC V7	SPARC V8 LEON 3FT	SPARC V8 LEON 3FT	SPARC V8 LEON 3FT
Clock Frequency	66 MHz	100 MHz	25 MHz	15 MHz	25 MHz	25 MHz	25 MHz
MIPS	53	86	20	12	25	25	25
Cache Size	8k Inst 8k Data	32k Inst 16k Data	NONE	NONE	8k Inst 4k Data	8k Inst 4k Data	8k Inst 4k Data
Floating Point	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SpaceWire	4	0	0	0	0	0	3
PCI	Yes	Yes	No	No	No	No	No
CAN	2	0	0	0	1	0	0
Ethernet	1	0	0	0	0	0	0
1553	0	0	0	0	1 RT	2 BC/RT/MT	0
Core Voltage I/O Voltage	2.5V 3.3V	1.8V 3.3V	5V 5V	3.3V 3.3V	1.5V 3.3V	1.5V 3.3V	1.5V 3.3V
Package	352 CQFP 484 CLGA	349 MCGA	256 MQFPF	256 MQFPF	352 CQFP	352 CQFP	624 CCGA

# GR-CPCI-UT699 LEON 3FT Evaluation Board

AEROFLEX

- ▼ Evaluation board available from Aeroflex Gaisler
  - System clock speed of 66Mhz
  - cPCI form factor and standalone bench-top configuration

