



March 2009

SOS13



# Memory Update

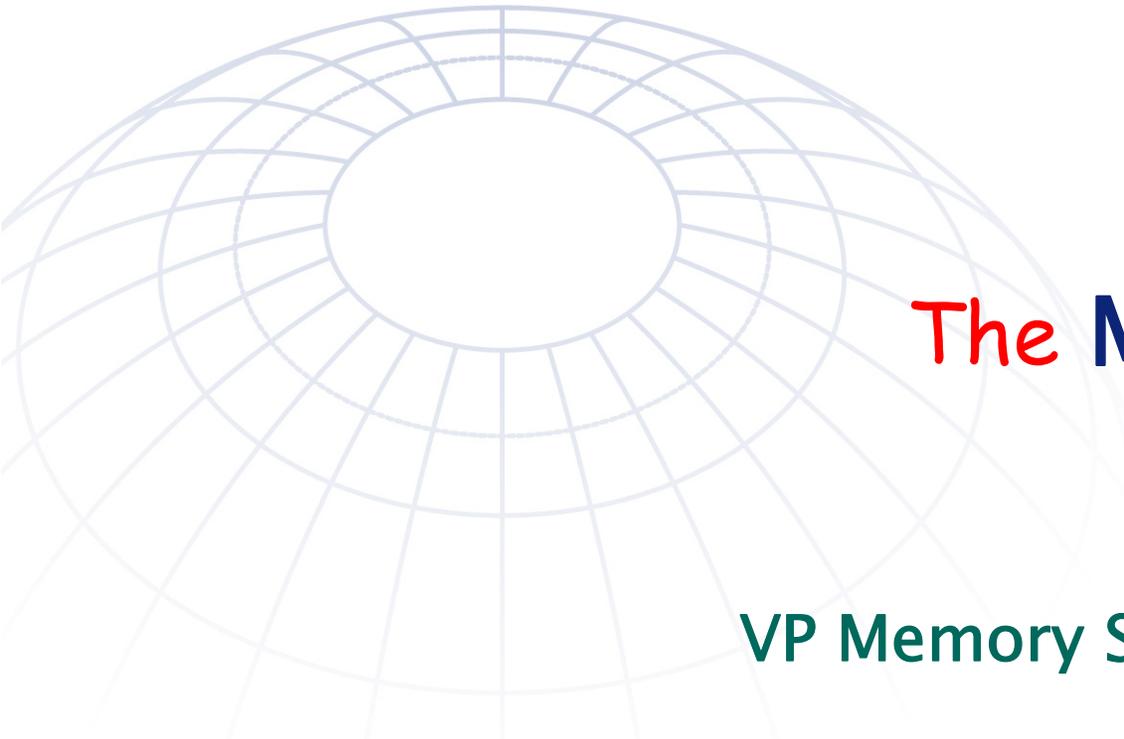
**Dean A. Klein**  
VP Memory System Development





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**Business**  
**The Memory Sucks**

**Dean A. Klein**  
**VP Memory System Development**



# Topics

- ▶ Memory Directions
- ▶ Memory Challenges
- ▶ Memory Opportunities

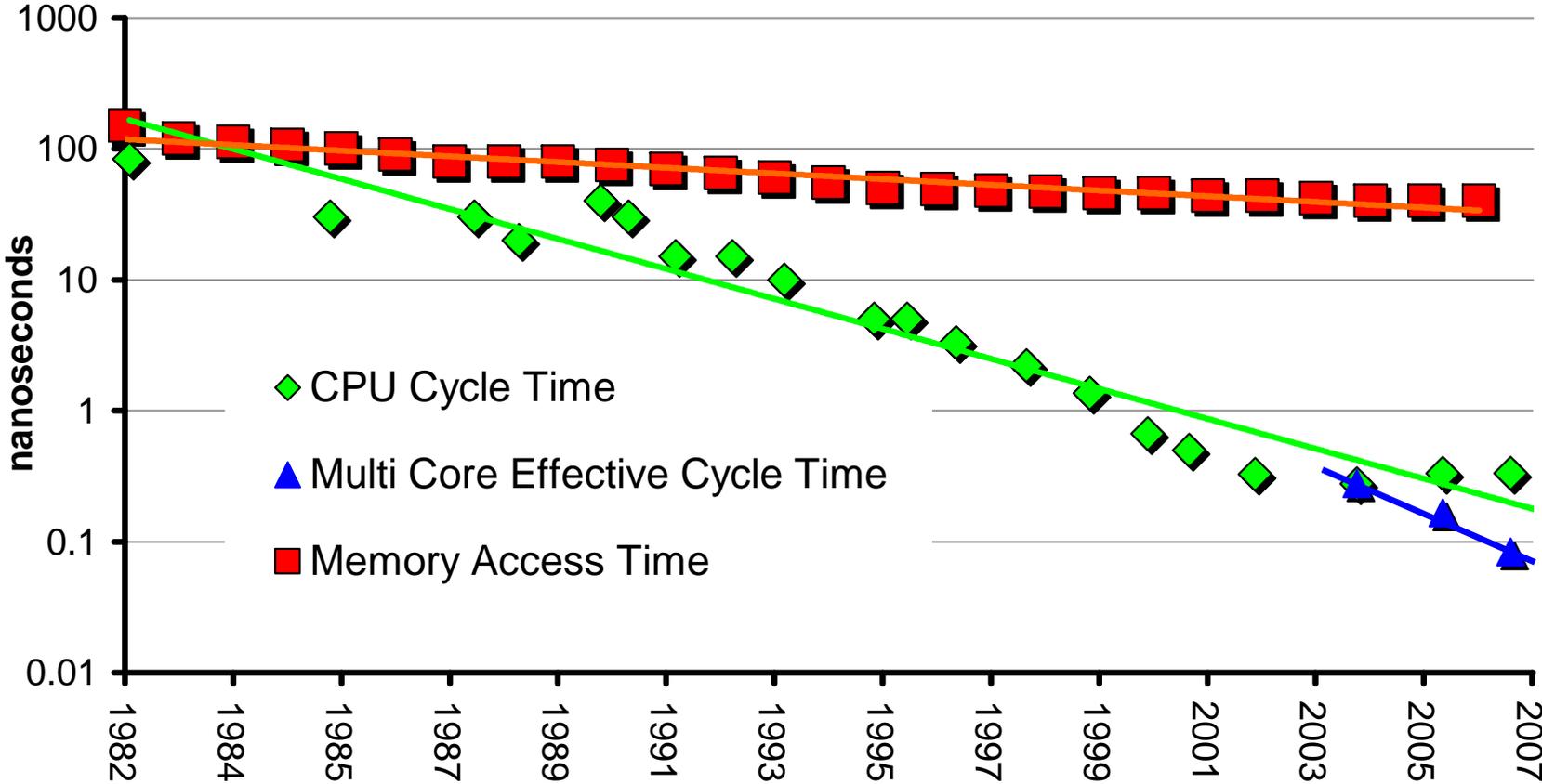


# The Results of Commoditization

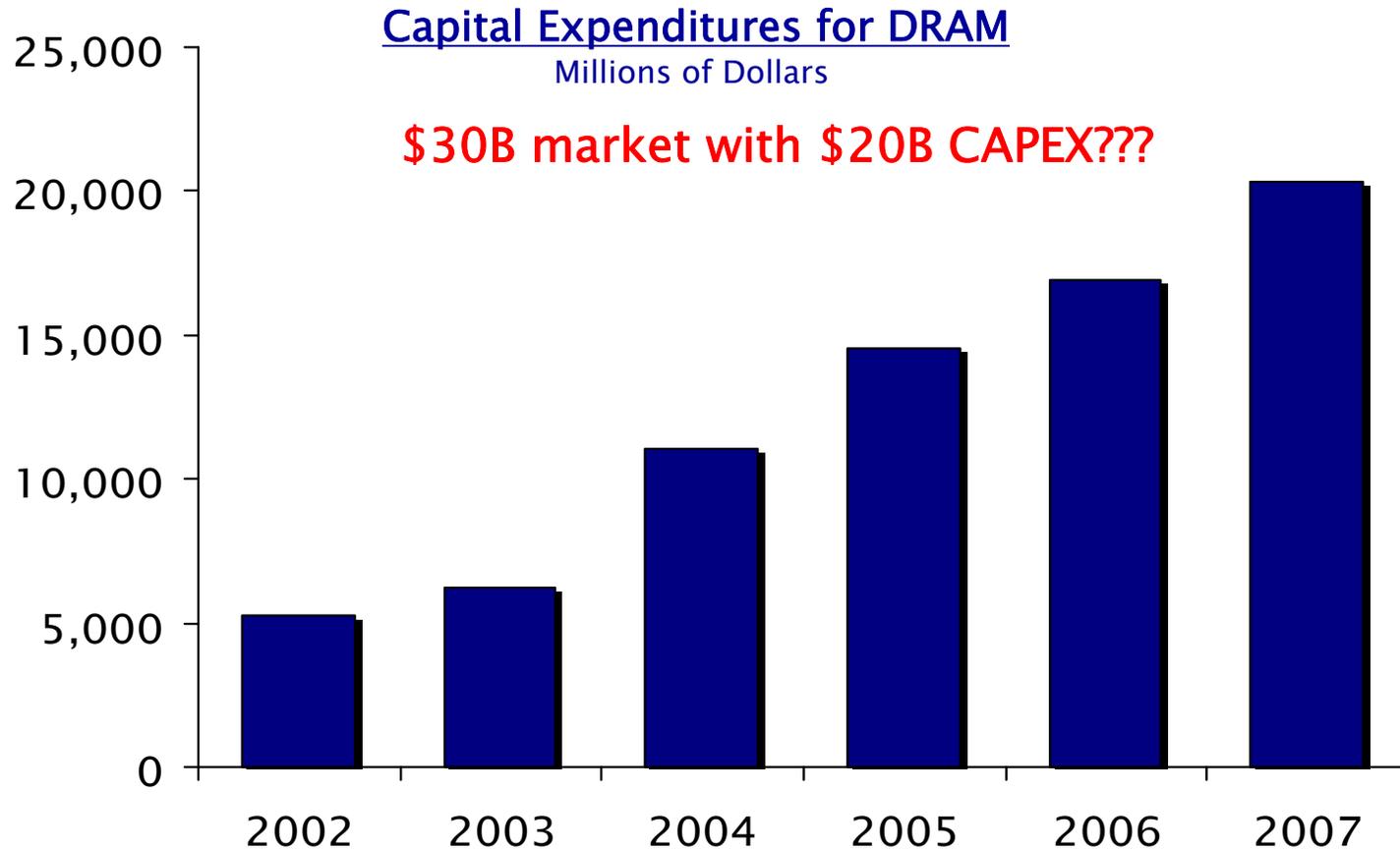
- ▶ Evolutionary development
  - PM, FPM, EDO, SDRAM, DDR, DDR2, DDR3...DDR4
  - Rare detours: RDRAM, BEDO, SLDRAM
  - Niche apps: RLDRAM, PSRAM, LP
- ▶ 40%/year average bit growth
- ▶ Cyclical
- ▶ Consolidating



# Evolution, not Revolution



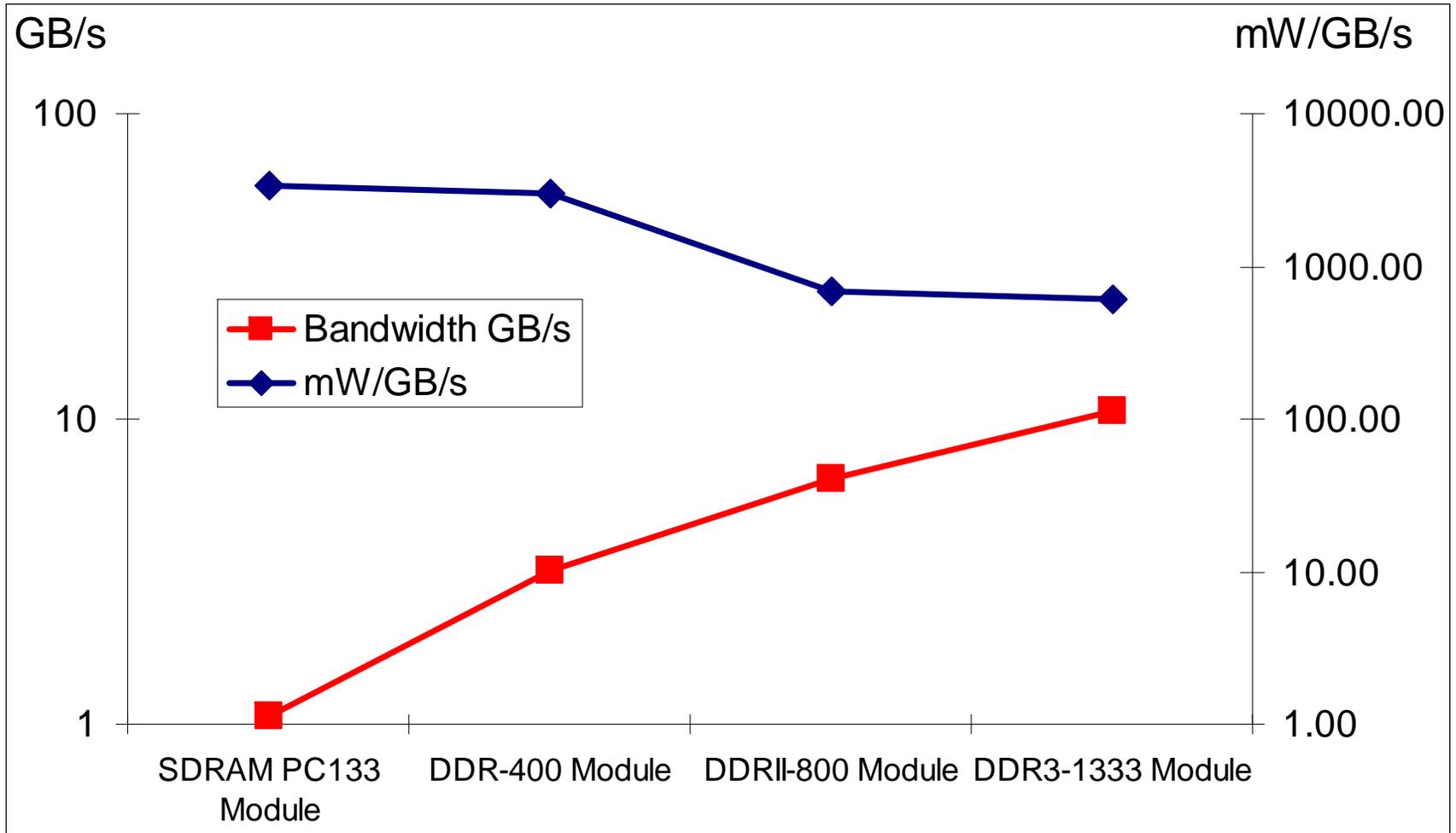
# Research Firm iSuppli Estimates that Roughly \$20Billion was Spent on DRAM Capex in 2007



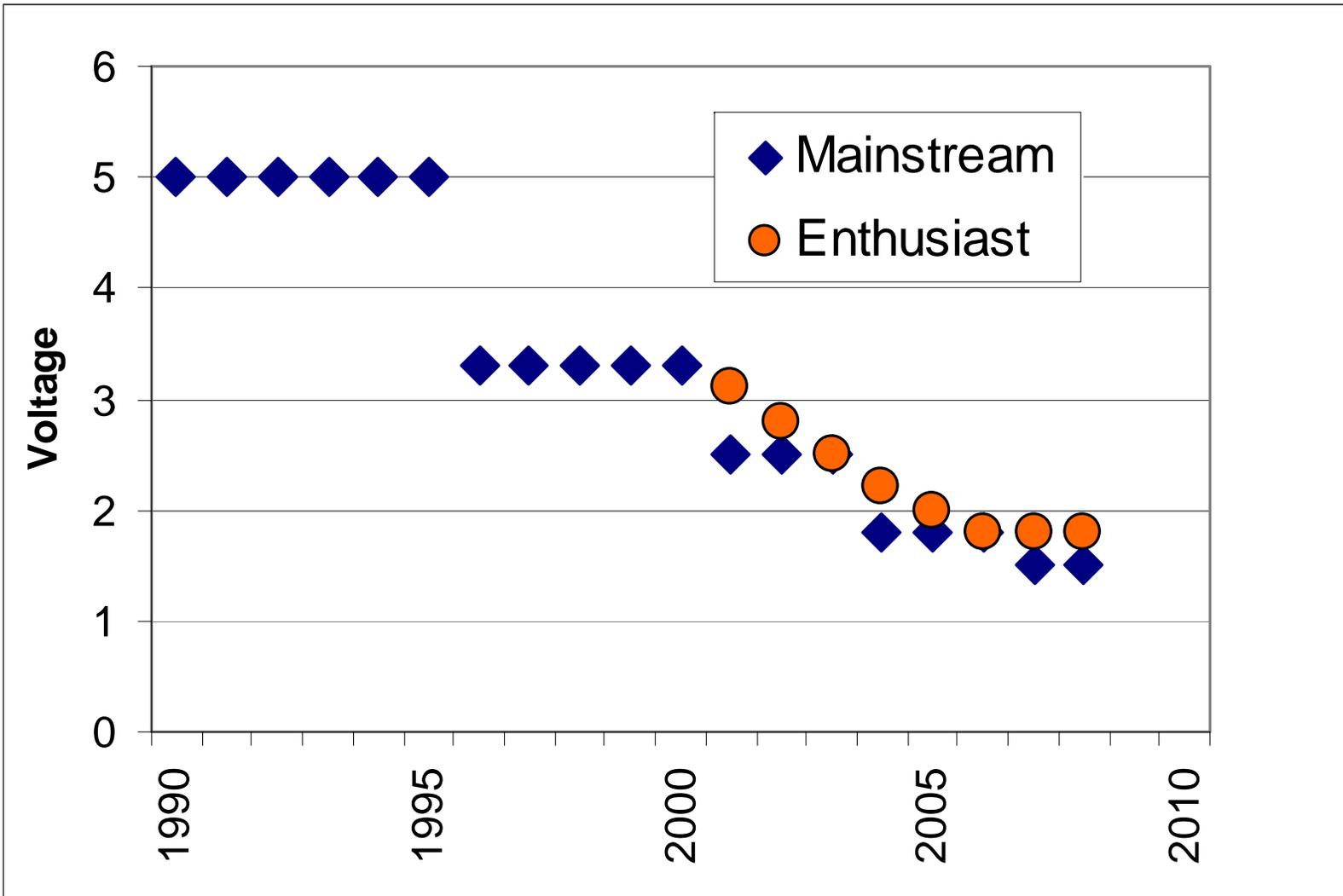
Source: iSuppli



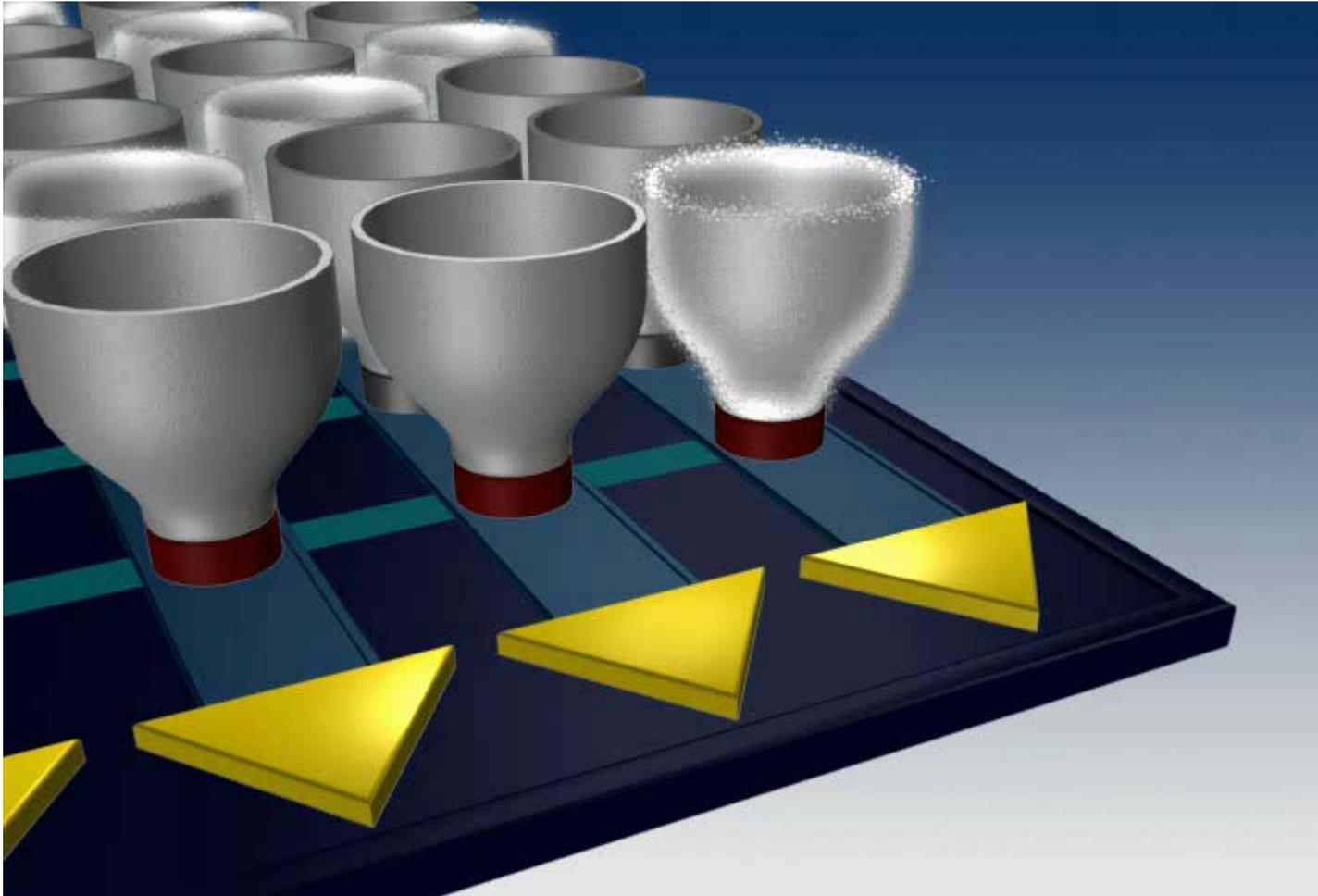
# Power and Bandwidth Trends



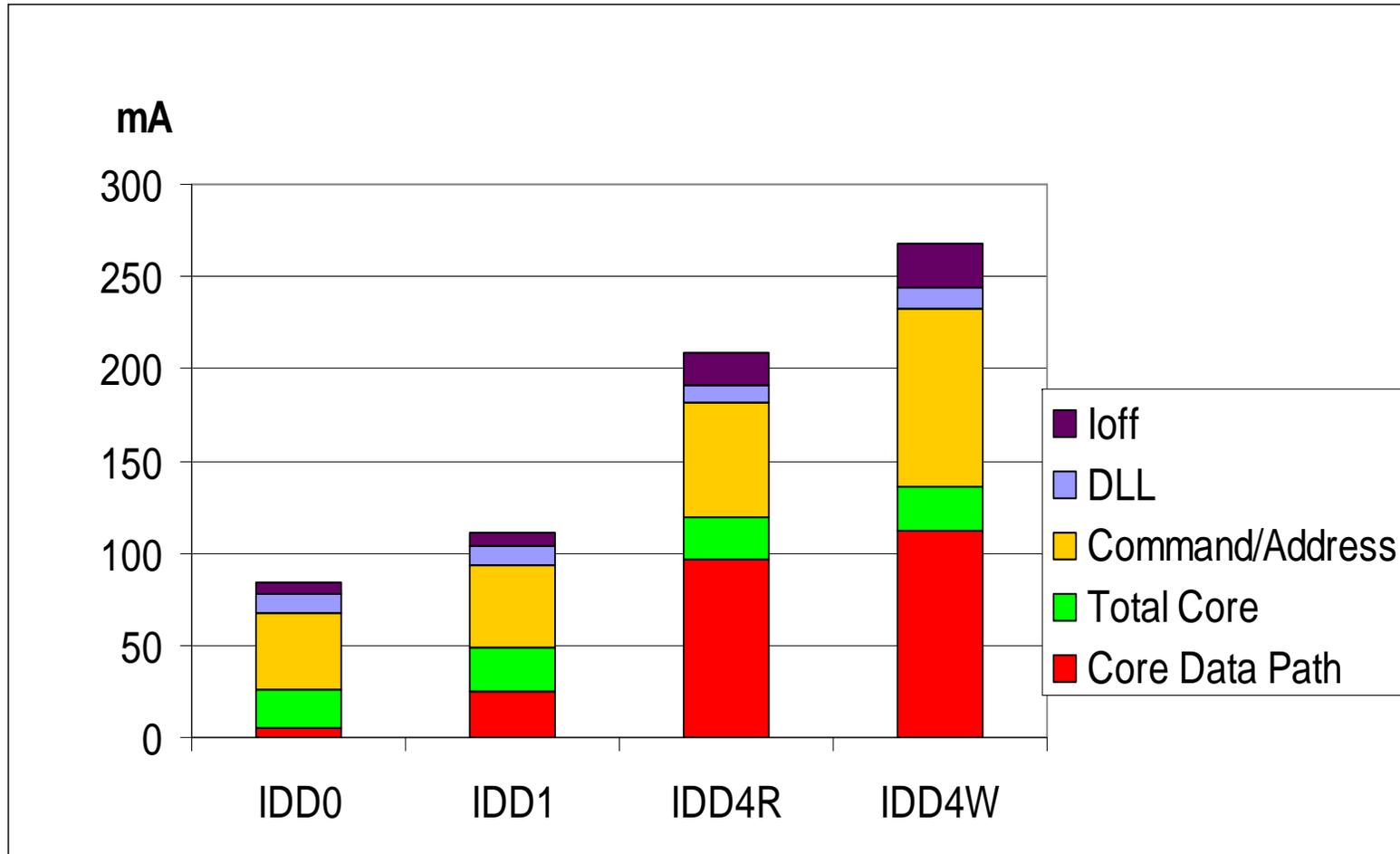
# Voltage Scaling Trend



# Underlying Physics



# Where's the Juice?



# DDR4 On Its Way. Hip, Hip...

## DDR4 JEDEC Status

- JEDEC pass/hold status including Feb. 2009 meeting

- › Voltage
  - VDD = VDDQ = 1.2V (baseline)
  - DDR4 will have lower active / idle power than DDR3 under same freq. and voltage (guideline)
- › Addressing (Bank Groups)
  - x4x8 supports 16 banks (4 groups of 4 banks each), x16 supports 8 banks (2 groups of 4)
  - 2Gb, 4Gb, and 8Gb densities defined
- › Addressing (Page Size)
  - x4 config (512 Byte page size), x8 config (1024 Byte page size), x16 config (2048 Byte page size)
- › Signaling

## DDR4 Task Group Discussions

- JEDEC Task Group discussions

- All Items are authorized to ballot in June 2009 if consensus reached
- › Voltage
  - 1.1V and 1.0V

## DDR4 Task Group Discussions (Cont.)

- JEDEC Task Group discussions (Cont.)

- All Items are authorized to ballot in June 2009 if consensus reached
- › Features/Functions
  - Data Mask protocol definition (no pin)
  - Data Bus Inversion (DBI)
  - 10UI CRC for data bus and error handling
  - Address/Command parity function and error handling
  - Address/Command latency function (power savings)
  - Boundary Scan
  - Single load memory stack
  - Fast-exit Self Refresh
  - DLL on/off modes
  - TCSR; granularity and "disable" mode
  - Temperature controlled auto-refresh
  - Implicit precharge function

- › Power voltage and frequency scaling (DVFS)
- › Migration roadmap

8GB density definition  
4 discussion

Stable for READs and WRITEs  
and/or on-die generation

MM, RDIMM/LRDIMM module pin count and dimensions

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# What to do???!!!

- ▶ Start a revolution?



3/17/2009

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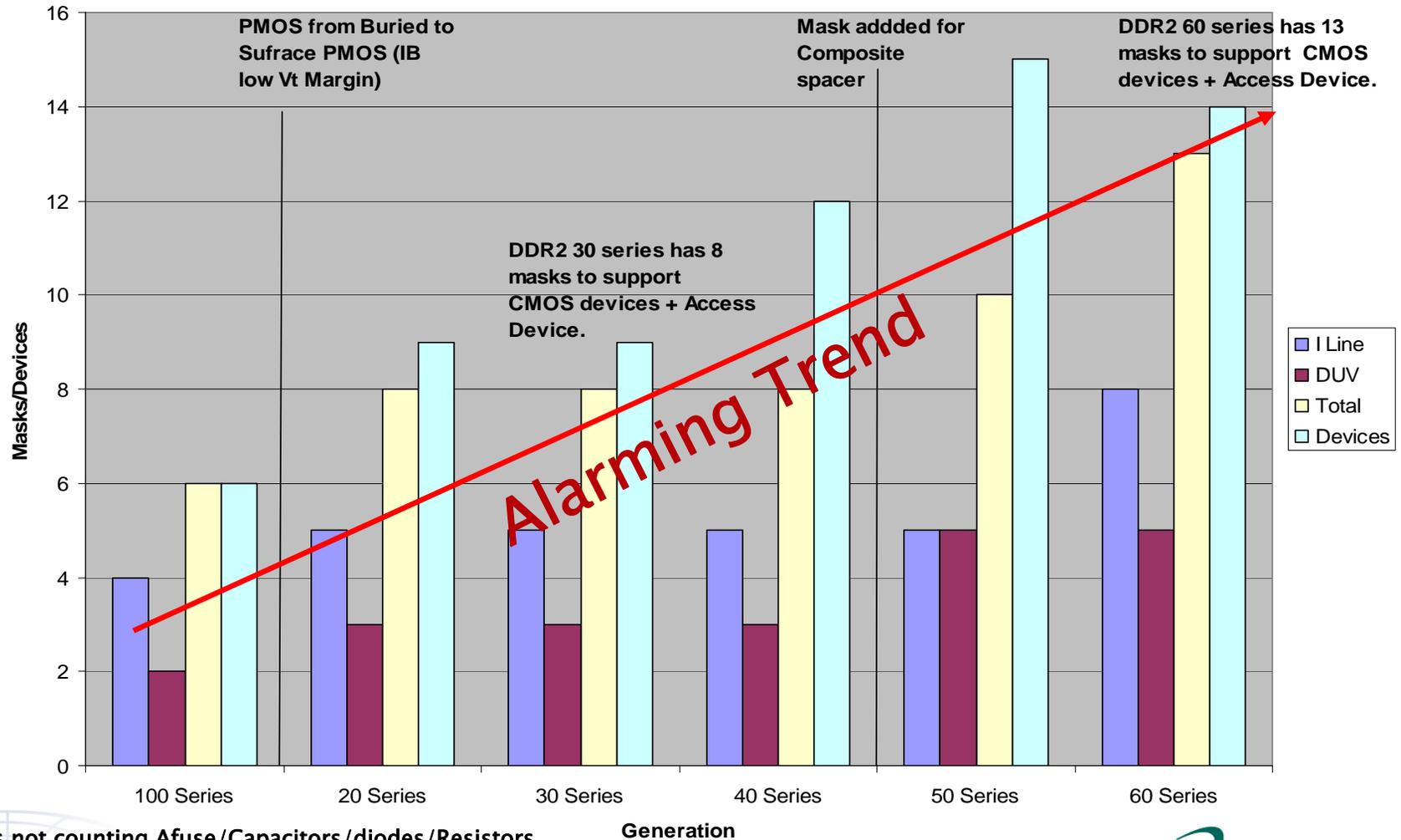
# What to do???!!!

- ▶ Start a revolution!
- ▶ Get close to the CPU
- ▶ Unlock internal bandwidth
- ▶ Allow concurrency
- ▶ Cut power dramatically



# Transistor Mask Count and Device Support

Transistor Masks vs. Generation



Source: KPAREKH

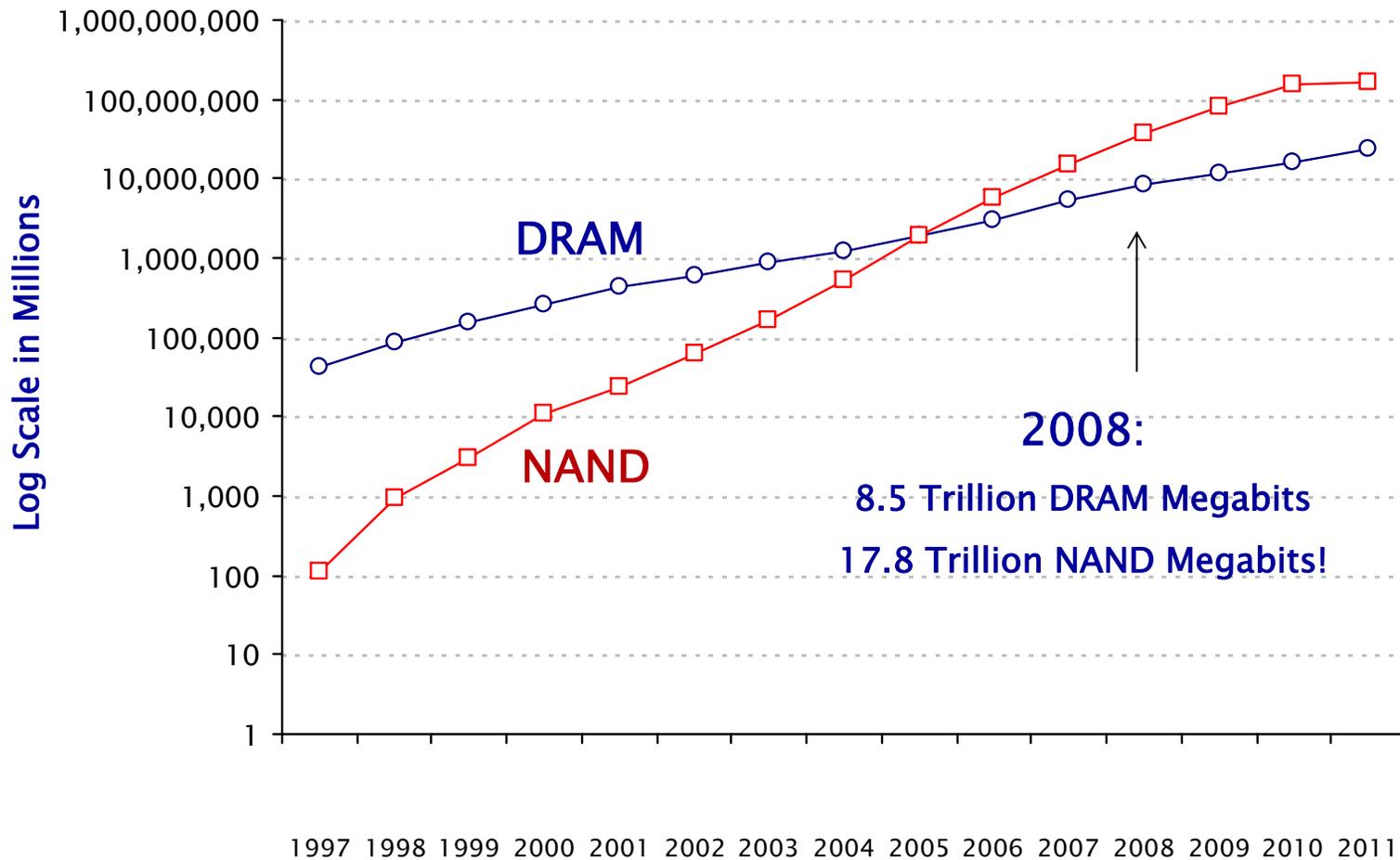
# The Role of NAND

- ▶ Low cost bits
- ▶ Can we live with the warts?
  - Endurance
  - Speed (Lack of)
  - Block Architecture
- ▶ Will it stick around?



# NAND Overtook DRAM in 2005 for Total Bits Shipped

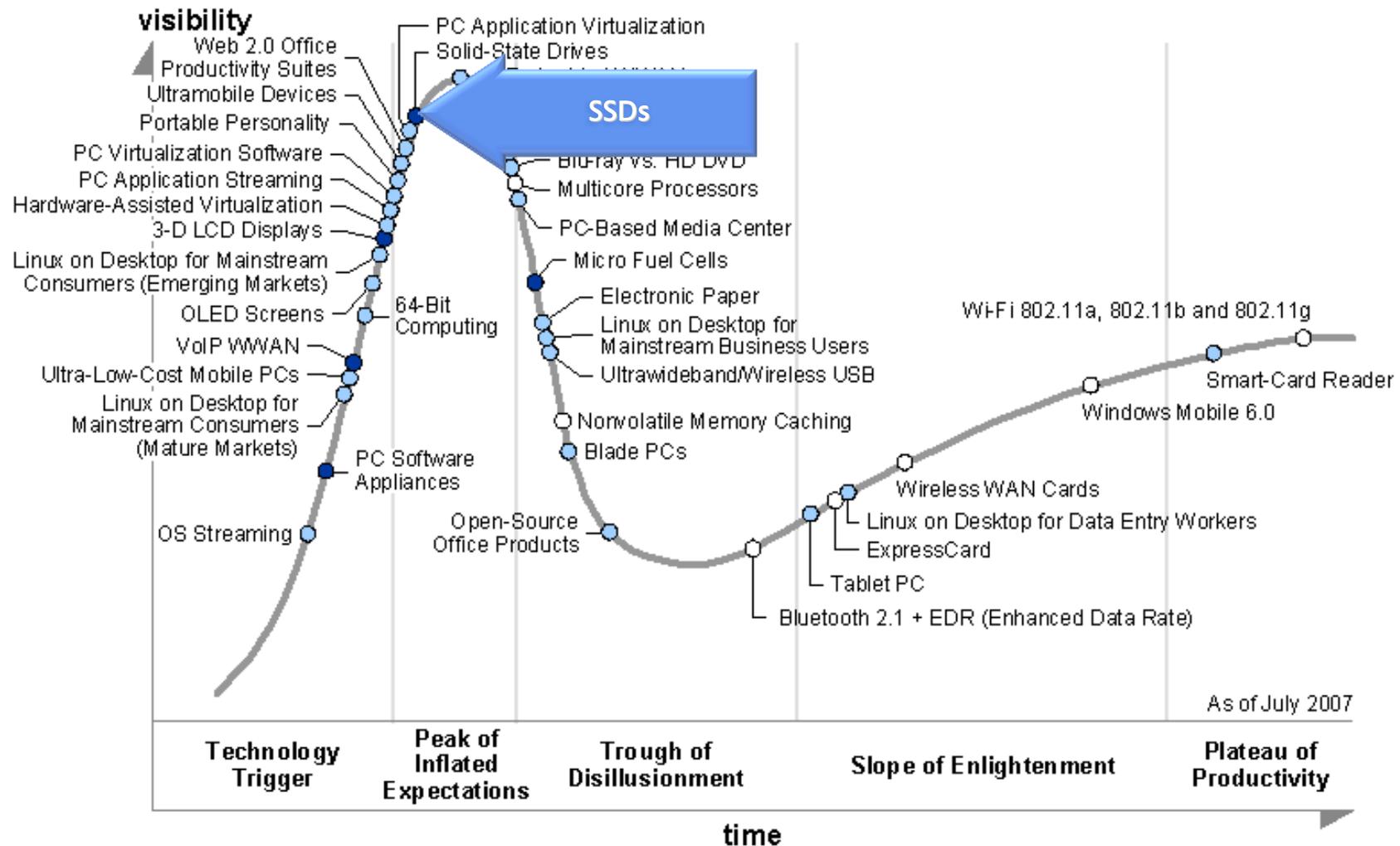
DRAM & NAND Megabits Shipped  
Millions of Megabits



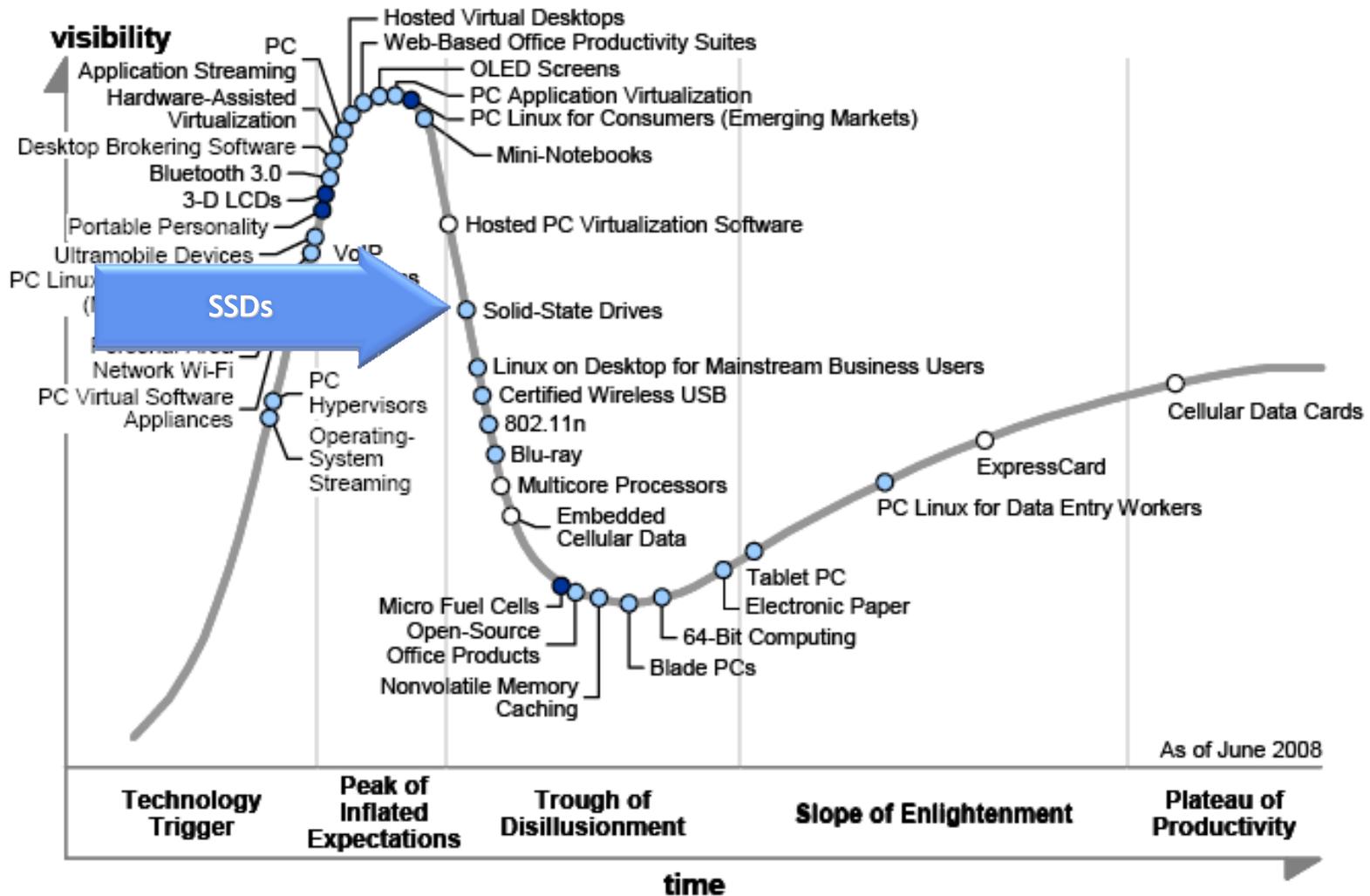
Source: Gartner



# Gartner's Hype Cycle for PC Technologies 2007



# Gartner's Hype Cycle for PC Technologies 2008



Years to mainstream adoption:

○ less than 2 years

● 2 to 5 years

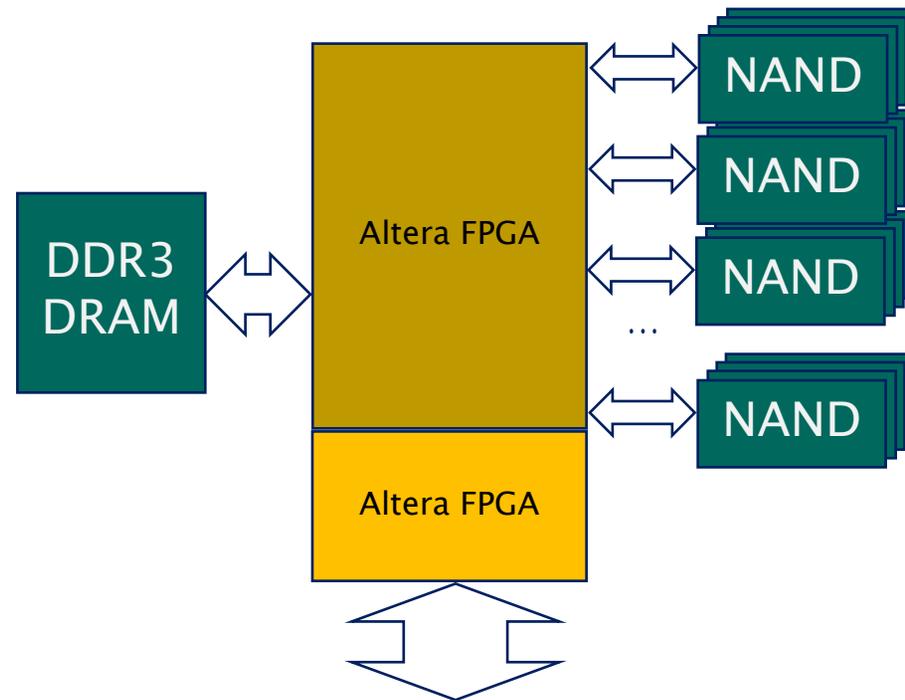
● 5 to 10 years

▲ more than 10 years

⊗ obsolete before plateau

# “Washington” Architecture Demo

- ▶ PCIe X8 Gen 1
  - ▶ 16 channels ONFI2.1 NAND, 128GB total
  - ▶ 1GB DDR3 DRAM
  - ▶ Two big FPGAs
- 
- ▶ 1.4GB/sec Read
  - ▶ 960MB/sec Write
  - ▶ >250K IOPS

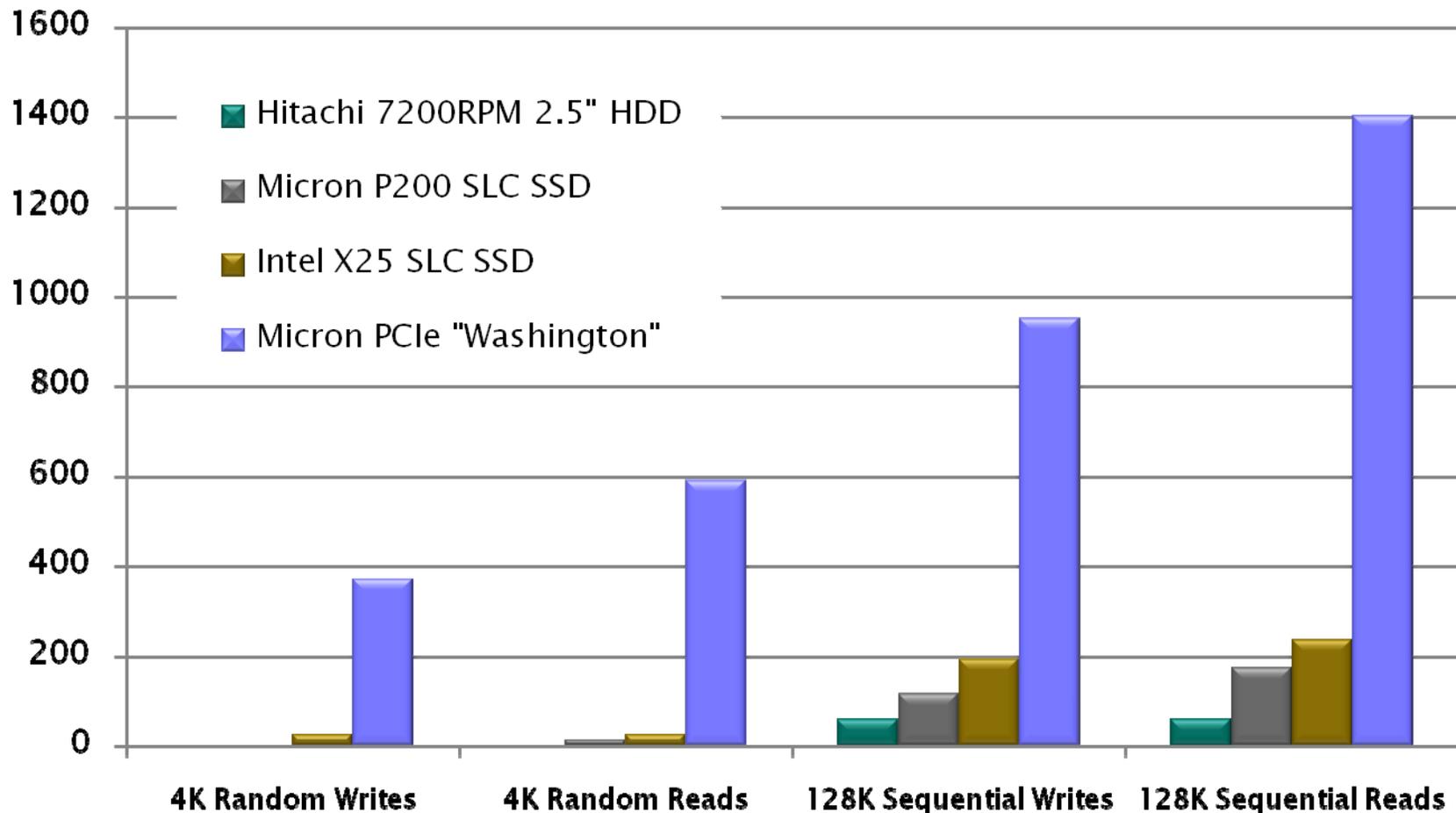


PCIe x8 Gen 1 (2GB/sec max)



# Washington vs. SSD/HDD

Bandwidth (MB/sec)



# Summary

Sell it at a loss, but make it up  
in volume...



# Summary

- ▶ Staying in the memory business requires huge amounts of capital.
- ▶ Success is never assured, due to supply/demand imbalance.
- ▶ Processes are getting more complex and expensive, as are the designs and the fabs.
- ▶ JEDEC serves memory customers.
- ▶ The memory hierarchy is expanding. NAND is the disruptor.





Questions?  
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