
Xyce™ Parallel Electronic Simulator Release Notes

Release 1.0

Scope/Product Definition

The Xyce™ Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The Xyce release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the Xyce web page at <http://www.cs.sandia.gov/xyce>.

Hardware/Software Information

This section gives basic information on supported platforms and hardware and software requirements for running Xyce 1.0.

Supported Platforms

Xyce 1.0 currently supports any of the following operating system (all versions imply the earliest supported - **Xyce** generally works on later versions as well) platforms:

- SGI IRIX® 6.5.2 (serial and parallel using SGI MPI 3.3)
- Redhat Linux®, version 7.1 on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Sun Microsystems Solaris 8.0, on UltraSPARC™ and later architectures (serial)
- Tru64 on HP Alpha® (serial and parallel)
- FreeBSD on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Microsoft Windows® (serial)

Build Capability but Not Supported

- CPlant™ on hp Alpha® (serial)

Hardware Requirements

The following are *estimated* hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum - *memory requirements increase with circuit size*
- 200MB disk space

Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required *to build Xyce* on a platform. These are *only* required when building **Xyce** from source. These are:

- Epetra, AztecOO (part of the Trilinos Solver Library, Sandia) and associated libraries (libepetra.a, libaztecOO.a, libifpack.a, libmachdep.a, liby12m.a, libzoltan_cpp.a (parallel only))
- SuperLU (<http://www.nersc.org>) (libepetra_sl_u.a. libsuperlu.a)
- Kundert Sparse (libepetra_sparse.a)

For parallel builds, the following are additionally required:

- MPI (<http://www-unix.mcs.anl.gov/mpi/>) library for message passing (version 1.1 or higher), such as MPICH or LAM

- **Zoltan** (Sandia, <http://www.cs.sandia.gov/Zoltan>) and its associated libraries (libzoltan.a, libparmetis.a, libmetis.a)
- **Chaco** (Sandia, <http://www.cs.sandia.gov/CRF/chac>) (libchaco.a, libChacoCPP.a (Xyce-version))
- libblas.a, liblaspac.a
- Gnome XML C library libxml2.a
- CoMeT Data Management library (libCDM.a)

Xyce™ Release 1.0 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. As this is the initial Version 1.0 release, some of this documentation is in “Draft” mode and is incomplete.

- **Xyce™** User’s Guide, Version 1.0
- **Xyce™** Release Notes, Version 1.0
- **Xyce™** Theory Document
- High Performance Electrical Modeling and Simulation Software Normal Environment Verification and Validation Plan, Version 1.0
- High Performance Electrical Modeling and Simulation Software Normal Environment Verification and Validation Plan Self Assessment, Version 1.0
- **Xyce™** Test Plan

New Features and Enhancements

Highlights

This release marks the first official release of Sandia’s **Xyce™** Parallel Electronic Simulator. Version 1.0 is a release that has obtained enough capability, stability and performance to be competitive with and, in some areas, outperform existing circuit simulation tools available from a variety of venues.

Since the last beta release, a myriad of enhancements and bug fixes have been made. These include changes to a new set of defaults for improved performance, new devices and improved user interactivity. Highlights for this release are:

- New default sparse-direct linear solver (KSparse) for improved performance on small circuits.
- Radiation (prompt photocurrent) aware diode model.
- Support for Sun Microsystems' Solaris systems (serial) in addition to the large number of supported platforms.
- XML metadata-based parser that allows for better integration with external tools by providing a common source for device data and parameters.
- New install and running scripts that install the **Xyce** executable, documentation and supporting XML files in appropriate locations. Additionally, **Xyce** is now run using a script that sets the run-time environment. Furthermore, the parallel version uses such scripts to wrap the MPI calls for the appropriate installation.
- Addition of Lambert-W function as an option for diode and bipolar transistor devices. When this option is enabled, Lambert-W functions are used in place of exponential functions. Generally, this results in greater numerical robustness for notoriously hard-to-solve devices.

Specific Features and Enhancements

Here we give the list of new supported features and enhancements for **Xyce**. For details of each of these options statements, see the **Xyce™** User's Guide.

New Device Support

- Radiation-aware (prompt-photo current) diode model.
- Support for PDE-devices which may be coupled with a larger analog circuit.

The complete device list is given in the table below:

Device	Comments
Resistor	Semiconductor
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductance (see below)
Diode (Level 1)	
Diode (Level 3) - radiation aware	Prompt photocurrent radiation model.
VCVS (voltage controlled voltage source)	3f5 compatible
VCCS (voltage controlled current source)	3f5 compatible
VSRC (independent voltage source)	
ISRC (independent current source)	
Bipolar Junction Transistor (BJT)	
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (BSIM3)	
VSWITCH	
Nonlinear Mutual Inductor	Sandia core model (not fully PSpice compatible)
Lossless Transmission Line	
BSRC (behavioral modeling source)	Digital primitives not yet supported
PDE Devices	Both 1D and 2D drift-diffusion models of semiconductor devices are available, though not officially supported. Official support for these devices will accompany the next release.

Robustness Improvements

- Improved time-integration and nonlinear solver default tolerances improve robustness.

Performance Improvements

Performance enhancements in this release (including the use of the Sparse solver) account for an approximately 40% speed improvement for small

circuits (~100 devices) in serial computations. The specific improvements include:

- New default sparse-direct linear solver (KSpase) for improved performance on small circuits in serial. The previous default sparse-direct linear solver (SuperLU) is still available as a netlist option and generally performs better on larger circuits (more than 1000 devices). To use this solver, set the KSpase flag to “0” in the netlist:

Example: `.OPTIONS LINSOL kspase=0`

- Direct-access matrices (*not on by default*) and vectors (*on by default*) for load calculations. To utilize the direct-access matrix feature, use the “-dma on” command line option:

Example: `> runxyce -dma on netlistname.cir`

- Other miscellaneous internal code optimizations.

Interface Improvements

- XML metadata-based parser that allows for better integration with external tools by providing a common source for device data and parameters.
- New run-time output. In transient mode, the “percent-complete” and “time-to-completion” is output to command line. In addition, the output can be stored in a log file via a command line option (see below).
- Xyce’s output (stdout) can be redirected to a log file by specifying `-l <logfile>` on the command line:

Example: `> runxyce -l output.log netlistname.cir`

Platform Support

- Support for Sun Microsystems’ Solaris systems (serial) in addition to the large number of supported platforms.
- Parallel support for hp AlphaServer Tru64 Unix systems in parallel (previously, this platform was only supported in serial mode).

Miscellaneous

- New install and running scripts that install the Xyce executable, documentation and supporting XML files in appropriate locations. Additionally, Xyce is now run using a script that sets the run-time environment. Furthermore, the parallel version uses such scripts to wrap the MPI calls for the appropriate installation.

Defects Fixed in this Release

Defect	Description
Core dump for BSRC using expression with zero explicit variables.	Xyce was failing when there were zero explicit variables in a Bsrc expression. This has been fixed.
Time-dependent Bsrc expression was ignored.	An expression had to be explicitly checked to see if it is time dependent. The parser did not make this check. In the B-source case, if the expression was only time-dependent, the parser did not detect it and evaluated it to a constant. This has been fixed.
Voluminous output from N_DEV_Device::updateTimeDependentParameters.	Errant output has been removed.
Inductor with core material properties not properly supported.	An inductor query was improperly excluding the case of one inductor listed in the K line with a nonlinear model. This has been remedied.
Restart problems on complicated circuits.	Xyce was failing to load restart files properly for some circuits. This has been fixed.
Nonlinear mutual inductance did not work in parallel.	This has been fixed and tested.
Some hyperbolic functions caused convergence problems.	Improvements in handling these have resulted in all test cases working properly.

Known Defects and Workarounds

Defect	Description
DC Sweep output.	DC sweep calculation does not automatically output sweep results <i>Workaround:</i> Use .PRINT statement to output sweep variable results.
Attempting to print the voltage for a non-existent node does not cause a warning.	Be careful. Make sure all requested output nodes exist.
Missing polynomial order in Bsrc "poly" statement causes Xyce to core dump.	Make sure Bsrc "poly" statement syntax includes polynomial order.
Not recognizing invalid netlist files.	Xyce will not recognize when a given netlist file is invalid. It will parse the file (whatever it is) and proceed to hang. <i>Workaround:</i> Ensure the last argument on the command line is a valid netlist file.

Failure for netlists using ChileSPICE digital primitives.	Xyce does not currently support the use of digital primitives.
Specifying a .TRAN analysis statement and a .PRINT DC statement will cause Xyce to core dump.	This is an invalid netlist which should be caught by the parser but currently isn't. <i>Workaround:</i> Don't specify invalid combinations in the netlist.
Xyce will not accept string parameters in models.	<i>Workaround:</i> Use integer for these values instead.

Incompatibilities With Other Circuit Simulators

Issue	Comment
.SAVE does not work	Xyce does not support this. Use .PRINT instead.
.OP is incomplete	A .OP netlist will run in Xyce , but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero	A requested pulsed source rise/fall time of zero really is zero in Xyce . In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand	Output variables have to be specified as V(node) or I(source). Just putting node alone will not work.
BSIM3 level	In Xyce the BSIM3 is level=9. Other simulators have different levels for the BSIM3.
Node names vs. device names	Currently, circuit nodes and devices MUST have different names in Xyce . Some simulators can handle a device and a node with the same name, but Xyce cannot.
Inline comments	Xyce does not support semi-colon delimited inline comments.
Interactive mode	Xyce does not have an interactive mode.
Time integrator default tolerances	Xyce has much tighter default solver tolerances, and thus takes smaller time steps. When this happens, it will take a larger total number of time steps for a given time interval. To have Xyce take time steps comparable to those of SPICE, set RELTOL and ABSTOL time integrator options to larger values (e.g., .OPTIONS TIMEINT RELTOL=5.0E-3 ABSTOL=1.0E-6).
ChileSPICE-specific "operating point voltage sources"	These are not currently supported within Xyce .

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