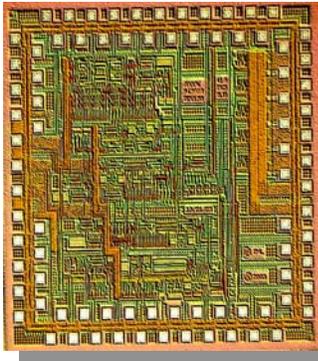




Xyce™ Simulation of the Spock ASIC

In November 2003, the Xyce™ (<http://www.cs.sandia.gov/Xyce>) team at Sandia National Laboratories further demonstrated the power of its modern solution methods



by performing a simulation of the W80-3 SA3989 (A.K.A. Spock) Firing-Set Application Specific Integrated Circuit (ASIC). The chip is being designed and manufactured by the MDL for the W80-3 Firing Set. This ASIC is a mixed-signal multi-function DC-to-DC power supply controller chip; it is comprised of approximately 4500 transistors; and is fabricated in the MDL CMOS6R radiation hardened process.

Steve Dunlap, the ASIC designer, used Xyce™ as a tool in his design and states that:

“Instrumental in the successful design of the SA3989 was the ability to conduct a pad-to-pad simulation of the part prior to manufacture, this insures that major design blocks internal to the ASIC interoperate correctly. Because of the analog components, size of the chip and its complexity the currently used design tools—PSPICE in particular—were not capable of performing this simulation. Attempts were made to run the pad-to-pad simulation on PSPICE, one simulation ran for 5 days on 550 MHz PC and only completed 30% before it failed. Interestingly, not only did the simulation fail to complete but upon examination of the data it was discovered that the simulation had produced erroneous output due to accumulated errors. Xyce™ was employed for the same purpose of performing a pad-to-pad simulation. Xyce™ required a great deal of custom “tweaking” but was able to complete the simulation, giving the designer greater confidence that the design would work as intended therefore reducing design cycles and consequently costs.”

Of particular note are the complexity of these “mixed-signal” (digital/analog) problems and the difficulty of simulating them at the transistor level. The analog portion of the ASIC provides a challenge to any device simulator since analog circuits are intrinsically more difficult to simulate than purely digital circuits. When this is combined with the particular nuances of modeling the digital components, the robustness of the underlying numerical algorithms of the application is significantly stressed. However, unlike many commercial circuit simulators, **Xyce** relies on state-of-the-art solution methods such as those included in the **Trilinos** solver suite (see below). Particularly crucial in this simulation were the **Xyce** time integration and step-size control methods as well as the **NOX** nonlinear solver library. The ability to “tune” these solvers allowed **Xyce** to run to completion and achieve the correct results for the critical DSW application.

About Xyce™

Xyce is a new circuit simulation code designed from the ground-up as a parallel tool in the most general sense, that is, a message passing parallel implementation, which allows it to run efficiently on the widest possible number of computing platforms. These include serial, shared-memory and distributed-memory parallel as well as heterogeneous platforms.

A DoE-ASC funded project, the **Xyce** Parallel Electronic Simulator development has focused on improving the capability over the current state-of-the-art in the following areas:

- Capability to solve extremely large circuit problems by supporting large-scale parallel computing platforms (up to thousands of processors). Note that this includes support for most popular parallel and serial computers.
- Improved performance for all numerical kernels (e.g., time integrator, nonlinear and linear solvers) through state-of-the-art algorithms and novel techniques including homotopy algorithms for key device models.
- Support for modeling circuit phenomena at a variety of abstraction levels (device, analog, digital and mixed-signal) in a rigorous and tightly coupled manner, allowing

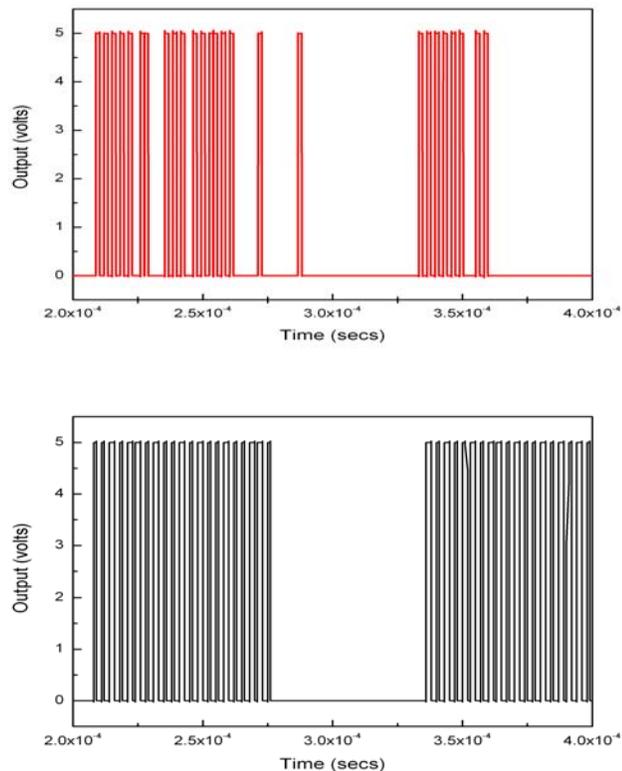


Figure 1. Comparison of erroneous Cadence PSpice (top) results with the correct Xyce™ (bottom) results for a key clocking signal.

for timely, full-system solutions. Furthermore, the development of environmentally “aware” (e.g., radiation) device models is a unique feature of the project.

■ Object-oriented code design and implementation using modern coding-practices that ensure that the **Xyce** Parallel Electronic Simulator will be maintainable and extensible far into the future.

■ Improved “usability” through improved analysis control (e.g., variable solution checkpoint/restart capability) that improves the design workflow.

For more information on **Xyce**, please visit <http://www.cs.sandia.gov/Xyce>

About Trilinos

The Trilinos Project is an effort to develop and implement robust, parallel, numerical solution algorithms using modern object-oriented software design, while still leveraging the value of established numerical libraries such as PETSc, Aztec, the BLAS and LAPACK. It emphasizes abstract interfaces for maximum flexibility of component interchanging, and provides a full-featured set of concrete classes that implement all abstract interfaces.

For more information on Trilinos, please see <http://software.sandia.gov/trilinos>

About NOX/LOCA

NOX is short for Nonlinear Object-Oriented Solutions, and its objective is to enable the efficient solution of nonlinear equations such as those arising in implicit PDE and DAE simulation codes. NOX is designed to work with any linear algebra package and to be easily customized. For more information, please see <http://software.sandia.gov/nox/>

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