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# Xyce™ Parallel Electronic Simulator Release Notes

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**Release 2.1**

Prepared by  
Sandia National Laboratories  
Albuquerque, New Mexico 87185 and Livermore, California 94550

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## Release 2.1

Eric R. Keiter, Scott A. Hutchinson, Robert J. Hoekstra, and Eric Rankin  
Computational Sciences

Thomas V. Russo, David N. Shirley, Phillip M. Campbell, and Carolyn W. Bogdan  
Component Information and Models

Sandia National Laboratories  
P.O. Box 5800  
Mail Stop 0316  
Albuquerque, NM 87185-0316

## Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at <http://www.cs.sandia.gov/xyce>.

## Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 2.1.

### Supported Platforms

**Xyce** 2.1 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 2.1 release.

- SGI IRIX® 6.5.3, Workshop Compilers 7.4.2 (serial and parallel using SGI MPI)
- Redhat Linux®, Enterprise version 9.0 on Intel Pentium® architectures (serial and parallel using MPICH version 1.2.5.2 or LAM MPI version 7.0.6)
- Tru64 on HP/Compaq Alpha® (serial and parallel)
- FreeBSD on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Microsoft Windows® (serial)
- Apple® OS X (serial)

### Build Capability but Not Supported

The platforms listed in this section are “not supported” in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 2.1 release. For large parallel platforms, such as ASCI White, this sort of testing is not a realistic option. These platforms are supported in the sense that **Xyce** 2.1 has been built for these platforms, and successfully executed on them. If a user needs to run **Xyce** 2.1 on one of these platforms, contact the **Xyce** team and we will work with you on a case-by-case basis.

- ASCI White (IBM) (parallel)
- Sandia Institutional Computational Clusters (serial and parallel).

## Hardware Requirements

The following are estimated hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*
- 50MB disk space (not including space needed for output files)

## Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required to build **Xyce** on a platform. These are only required when building **Xyce** from source. These are:

- Trilinos Solver Library (Sandia, <http://software.sandia.gov/Trilinos>) . This is a suite of libraries including Amesos, KLU, AztecOO, Belos, Epetra, EpetraExt, Ifpack, NOX, LOCA, and y12m.
- SuperLU (<http://www.nersc.org>)
- Xyce Expression library (libexpr.a).
- BLAS (libblas.a).
- LAPack (liblapack.a).

For parallel builds, the following are additionally required:

- MPI (<http://www-unix.mcs.anl.gov/mpi/>) library for message passing (version 1.1 or higher), such as MPICH or LAM. The version used to build Xyce must be the same that is used for building Trilinos.
- Zoltan (Sandia, <http://www.cs.sandia.gov/Zoltan>) and its associated libraries (libzoltan.a, libzoltanCPP.a, libparmetis.a, libmetis.a)

## Xyce Release 2.1 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. Some of this documentation is in Draft mode and is incomplete.

- **Xyce** Users' Guide, Version 2.1
- **Xyce** Reference Guide, Version 2.1

- **Xyce** Release Notes, Version 2.1
- **Xyce** Theory Document
- **Xyce** Test Plan

## New Features and Enhancements

This release is the first release following the Version 2.0 release. It encompasses many key bug fixes as well as key robustness and performance enhancements. Highlights for this release include:

- Improved parser scalability, achieved with a new ‘distributed’ parser.
- Updated to Trilinos solver library, version 4.0.
- Stability enhancements to the prompt photocurrent models and additional photocurrent models.
- Improved support for .STEP and .DC analysis, to include logarithmic sweeps.
- Enhanced MOSFET-based homotopy algorithms for DCOP solution.
- New device models: JFET, BJT-neutron, VDMOS, VDMOS-photocurrent
- More extensive support for TCAD devices (formerly referred to as “PDE” devices).

Note that the first two items represent a significant enhancement, particularly for parallel simulation using **Xyce**. For details of each of these new features, see the **Xyce** Users’ Guide, and the **Xyce** Reference Guide.

## Device Support

Table 1 contains a complete list of devices for **Xyce** Release 2.1. A number of the devices have been revised to improve robustness, and additional model levels (the level=3-4 BJT; the level=18-19 MOSFET) for some devices types have been added. One new device type, the JFET, is has also been added for **Xyce** Release 2.1.

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible)
Resistor	Semiconductor
Diode (Level 1)	

Device	Comments
Diode (Level 3)	Prompt photocurrent radiation model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Voltage Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT)(Level 1)	
Bipolar Junction Transistor (BJT)(Level 2)	Prompt photocurrent radiation model.
Bipolar Junction Transistor (BJT)(Level 3)	<b>New!</b> Neutron-effects model.
Bipolar Junction Transistor (BJT)(Level 4)	<b>New!</b> Alternate prompt photocurrent radiation model.
Junction Field Effect Transistor (JFET)	<b>New!</b> Level-1 JFET model.
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (Level 9)	BSIM3 model.
MOSFET (Level 18)	<b>New!</b> VDMOS model.
MOSFET (Level 19)	<b>New!</b> VDMOS photocurrent model.
Transmission Line	Lossless.
Voltage Controlled Switch (VSWITCH)	
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional

Table 1: Devices Supported by Xyce.

## Robustness Improvements

- The addition of homotopy algorithms has led to **Xyce** being much more robust for large MOSFET circuits.
- The radiation models (Level 3 Diode and Level 2 BJT) have been made less susceptible to roundoff error, and now support breakpoints for discontinuity capturing.

## New Device Types

- **Xyce** now supports the SPICE-compatible JFET model.

## New Model Levels

- Level 3 BJT, a neutron-aware BJT model.
- A level 4 BJT implementing the photocurrent effects of the level 2 BJT into the native Xyce BJT (Level 1). Tests have indicated that this is much more robust than the level 2 BJT in this or any previous Xyce release.
- Level 18 MOSFET model for double-diffused vertical power MOSFETS and a photocurrent model of the same, level 19.

## Enhanced Solver Stability and Features

- Xyce now uses Trilinos solver library version 4.0.
- A new serial-direct linear solver is available in **Xyce**, called KLU. This solver has been specifically designed for circuits. While it has not been made the default for **Xyce** 2.1, users are encouraged to try it, and it will probably be made the default in future **Xyce** releases.

## Interface Improvements

- The netlist parser has been optimized for large parallel runs.
- .DC and .STEP analyses now support stepping by octave, decade, and over a list of specified values.
- It is now possible to specify expressions to be printed on the .PRINT line in addition to voltage nodes and branch currents.
- Enhanced compatibility with PROBE format output files.
- Enhanced compatibility with Tecplot format output files.

## Defects of Release 2.0 Fixed in this Release

Defect	Description
Improper handling of non-numeric node names in B source. [Bug 428]	The parser and B source code have been repaired.
Improper handling of function definitions that did not use all arguments provided to function. [Bug 226]	Functions that do not use all of the provided arguments are now correctly parsed.
Level 3 diode crashes at end of run if CJO=0. [Bug 550]	A mistake in the device destructor was fixed.
Small circuits were causing parallel runs of Xyce to fail. [Bug 291]	Improved parallel support for small circuits. Xyce can more robustly handle small circuits in parallel, with far fewer limitations than in previous releases.
Incorrect handling of device initialization in .DC sweeps. [Bug 536]	Xyce was incorrectly re-initializing junction voltages at each step of a DC sweep, leading to unexpected behaviors. Code was changed to initialize those voltages only in the same way that SPICE does.
Square bracket usage in "Vector Composite" parameters results in incorrect parsing of netlists from other simulators. [Bug 425]	Square brackets are no longer used as delimiters for this type of parameter and are now allowed in node and device names.
Inappropriate nonlinear solver "searchmethod" parameter default. [Bug 402]	In Release 2.0 the default nonlinear solver search method was inappropriately chosen to be "Quadratic Line Search." This method is not well-suited for use with devices that use "voltage limiting" such as the BJT and MOSFET. In this release the default has been returned to "Full Newton."
Core dump when improper LOCA options specified [Bug 408]	The code now reports the error and exits cleanly.
Nonlinear solver allows transient to proceed even if DC operating point failed [Bug 354]	Under certain pathological circumstances the DC operating point would fail, but the nonlinear solver would return a failure flag that was not tested for. In these cases transient simulation would begin anyway and ultimately fail with error messages unrelated to the problem encountered. This has been fixed.
OFF parameter accepted by BJT but ignored [Bug 545]	The OFF parameter was not being used by the BJT code in the initialization of the device. It is now SPICE compatible.
Assorted parameter scoping problems [Bugs 534, 537, 604]	Several bugs in the handling of parameters local to a subcircuit were found and repaired.

Defect	Description
Memory leaks and missing error checking in expression library [Bug 547]	The expression library was leaking memory, and was also not checking to see if it was able to allocate memory before trying to use a requested block, leading to a core dump with no error message. The library now tests that it was able to perform an allocation before trying to use the allocated memory.
Segmentation fault when parsing subcircuit usage error [Bug 411]	<b>Xyce</b> was crashing with a segmentation fault if a subcircuit call was made with an incorrect number of nodes. The parser now checks for this error.
Parameters for .OPTIONS RESTART were case and order sensitive [Bug 524]	Unlike most .OPTIONS lines, the parameters for .OPTIONS RESTART were case sensitive and had to be specified in a precise order. This is no longer the case.
Expressions and parameters did not work inside “vector composite” parameters [Bug 573]	This has been fixed.
<b>Xyce</b> meaning of third parameter in .TRAN line inconsistent with meaning in SPICE [Bug 396]	In releases of <b>Xyce</b> prior to 2.1, the third parameter in the .TRAN line (“TSTART”) was used to indicate the time at which the simulation was to start. In SPICE it is the time before which to discard output. <b>Xyce</b> now uses this parameter in a SPICE-compatible manner. This can have a significant impact on circuits with charge storage elements, as previous versions of <b>Xyce</b> would not have run the early part of the transient to allow those devices to charge up.
Parse error when PULSEDATA parameter used for radiation-aware devices [Bug 410]	The PULSEDATA parameter was left out of the metadata distributed with <b>Xyce</b> Release 2.0. In addition, even when the missing line was reinserted into the metadata all parameters following the second double quotation mark around the file name were ignored. If the optional parentheses were used around the model parameters, this would lead to a parse error about a missing closing parenthesis. This bug was fixed.
Restart of netlists including transmission lines did not work [Bug 442]	<b>Xyce</b> was not saving all the data needed for the restart of netlists that include transmission line devices. This is now fixed.
CSD (FORMAT=PROBE) output for .STEP runs not PSPICE compatible [Bug 598]	The CSD output format has been improved in this release.
Incorrect and/or insufficient error reporting [Bugs 439, 601, 612]	Several parser related bugs in error handling and reporting are fixed.
Install fails but reports success [Bug 492]	Robustness of the installation routine for Microsoft Windows is improved.

Table 2: Fixed Defects.

## Known Defects and Workarounds

Defect	Description
.DC sweep output.	.DC sweep calculation does not automatically output sweep results. <i>Workaround:</i> Use .PRINT statement to output sweep variable results.
Failure for netlists using ChileSPICE digital primitives.	<b>Xyce</b> does not currently support the use of digital primitives.
BJT Current Crowding	“Timestep too small” failures can result when IRB nonzero with level 2 and level 4 BJT <i>Workaround:</i> If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the <b>Xyce</b> development team so that this bug can be characterized and eliminated.
Microsoft Windows installation restrictions	Users with insufficient privileges (i.e. Limited Account) are not permitted to install <b>Xyce</b> into folders on the System Drive (usually C:). <i>Workaround:</i> First, manually create the desired folder on the System Drive. It is then possible to install <b>Xyce</b> into this folder by following the standard Setup procedure.
MPICH parallel runs may not exit cleanly	<b>Xyce</b> may not exit cleanly if it encounters certain errors during parsing. <i>Workaround:</i> If <b>Xyce</b> appears to hang, manually terminate each process. Usually a SIGTERM or ^C is sufficient to halt the job. Users running on the Alpha should manually check for zombie processes after <b>Xyce</b> error exits, and kill them if necessary.
Incompatible proprietary file formats.	Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in <b>Xyce</b> . <b>Xyce</b> does not recognize proprietary file formats. <i>Workaround:</i> It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.
Apple OSX incompatible file formats	It is possible for some OSX editors to apply incompatible line terminators to netlists. This causes <b>Xyce</b> to hang. <i>Workaround:</i> Use an alternate text editor that is capable of saving the netlist in a UNIX or DOS format.

Defect	Description
<p>Memory leak for parallel use of SuperLU and KLU linear solvers</p>	<p>A memory leak exists when using either SuperLU or KLU linear solvers with the parallel version of <b>Xyce</b>.  <i>Workaround:</i> For DCOP runs and transient runs with a limited number of timesteps for small to moderate circuits, this defect should not be a problem since there is no memory corruption. For larger circuits and many timesteps, this defect could cause memory to be fill up. For these cases, AztecOO should always be used as the linear solver.</p>
<p>Data always all zeros in homotopy output files (*.cir.HOMOTOPY.prn).</p>	<p>This wasn't noticed until it was too late to fix for release 2.1. This capability is only relevant to the use of homotopy to obtain operating points, and is mostly a developer capability.  <i>Workaround:</i> If we have a patch release, this bug will be fixed for it. If this particular capability is needed before then, consult with the <b>Xyce</b> team to get a development branch binary of <b>Xyce</b>.</p>
<p>Capacitive terms in JFET are inaccurate.</p>	<p>This wasn't noticed until it was too late to fix for release 2.1. The issue is that the JFET is hardwired to use a first-order (Backward Euler) time integration scheme. Xyce uses Backward Euler by default, so under normal default conditions the error analysis and time stepping in Xyce will be correct. If one specifies a non-default time integration method, the code will not produce an accurate answer.  <i>Workaround:</i> To get the best accuracy for this device, transient JFET circuits should always be run using Backward Euler. This is the default, so the only workaround is for users to avoid specifying non-default time integration methods.</p>
<p>Expressions in the .PRINT line can't use variables specified by .PARAM statements.</p>	<p>Specifying expressions in the .PRINT line is a new <b>Xyce</b> capability. It is very useful, but is unable to use .PARAM variables.  <i>Workaround:</i> For now, the only solution is to not use .PARAM variables in .PRINT statement expressions. This will be fixed for a later release.</p>
<p>One known instance of restart results not matching original run results.</p>	<p>There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range.  <i>Workaround:</i> The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.</p>

Table 3: Known Defects and Workarounds.

## Incompatibilities With Other Circuit Simulators

Issue	Comment
.SAVE does not work.	<b>Xyce</b> does not support this. Use .PRINT instead.
.OP is not complete	A .OP netlist will run in <b>Xyce</b> , but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In <b>Xyce</b> the BSIM3 level=9. Other simulators have different levels for the BSIM3.
Node names vs. device names.	Currently, circuit nodes and devices <b>MUST</b> have different names in <b>Xyce</b> . Some simulators can handle a device and a node with the same name, but <b>Xyce</b> cannot.
Interactive mode.	<b>Xyce</b> does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources."	These are not currently supported within <b>Xyce</b> . <i>However...</i> <b>Xyce</b> does support "IC=<value>" statements for capacitors and inductors which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for .STEP is different.	The manner of specifying a model parameter to be swept is slightly different. Also, it is not possible to do a .STEP sweep over a global parameter. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

## Important Changes to Xyce Usage Since the Last Release.

Table 5 lists some usage changes for Xyce.

Issue	Comment
The linear solvers netlist specification has changed.	This was done as part of the upgrade to Trilinos 4.0. In previous versions of the Xyce, the linear solver was specified using a combination of options in both the .OPTIONS NONLIN statement, and the .OPTIONS LINSOL statement. This was confusing, and has been corrected. As a result, .OPTIONS NONLIN DIRECTLINSOL=flag is no longer valid, and .OPTIONS LINSOL KSPARSE=flag is also not valid. To specify a linear solver, use .OPTIONS LINSOL type=SolverName, where SolverName is a string, and can be set to klu, superlu, ksparse or aztecoo.
The linear solvers command-line specification has changed.	This is similar to the previous issue. It is now possible to set which linear solver is being used, from the command line. For details, see the Xyce Reference Guide.
The TCAD/PDE devices no longer use square brackets in the doping and electrode netlist specification.	This has been changed to curly brackets, to allow better netlist compatibility with other circuit simulators. [Bug 425]

Table 5: Changes to netlist specification since the last release.

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## Contacts

Bug Reports

<http://tvrusso.sandia.gov/bugzilla>

Email

[xyce-support@sandia.gov](mailto:xyce-support@sandia.gov)

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